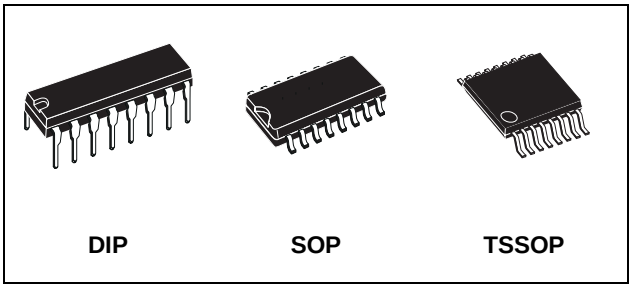
Beijing Relitech Co., LTD.

RD74HC595

8-BIT SHIFT REGISTER WITH OUTPUT LATCHES (3-STATE)

Datasheet- production data



DIP SOP TSSOP

Features

- HIGH SPEED:
  f_{MAX} = 59MHz (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 4μA (MAX.) at T_A= 25°C
- HIGH NOISE IMMUNITY:
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}|$ = I_{OL} = 6mA (MIN.) for Q_A to Q_H
  $|I_{OH}|$ = I_{OL} = 4mA (MIN.) for $Q_{H'}$
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC}(OPR.) = 2V to 6V

Applications

- AUTOMOTIVE
- INDUSTRIAL
- COMPUTER
- CONSUMER

Description

The RDHC595 device is a high-speed CMOS 8-bit shift register with output latches (3-state) fabricated with silicon gate CMOS technology.

This device contains an 8-bit serial in, parallel out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-state outputs. Separate clocks are provided for both the shift register and the storage register.

The shift register has direct overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

PART NUMBER	PACKAGE
RD74HC595BDI	DIP16
RD74HC595BSO	SOP16
RD74HC595BTS	TSSOP16

1 Pin information

Figure 1. Pin connection

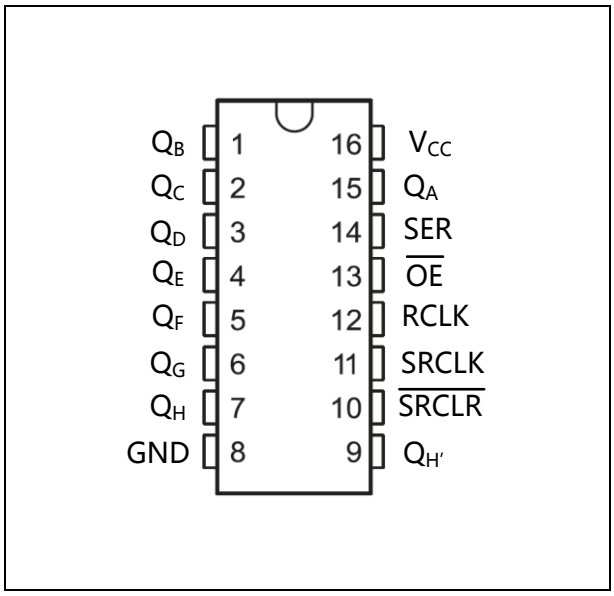
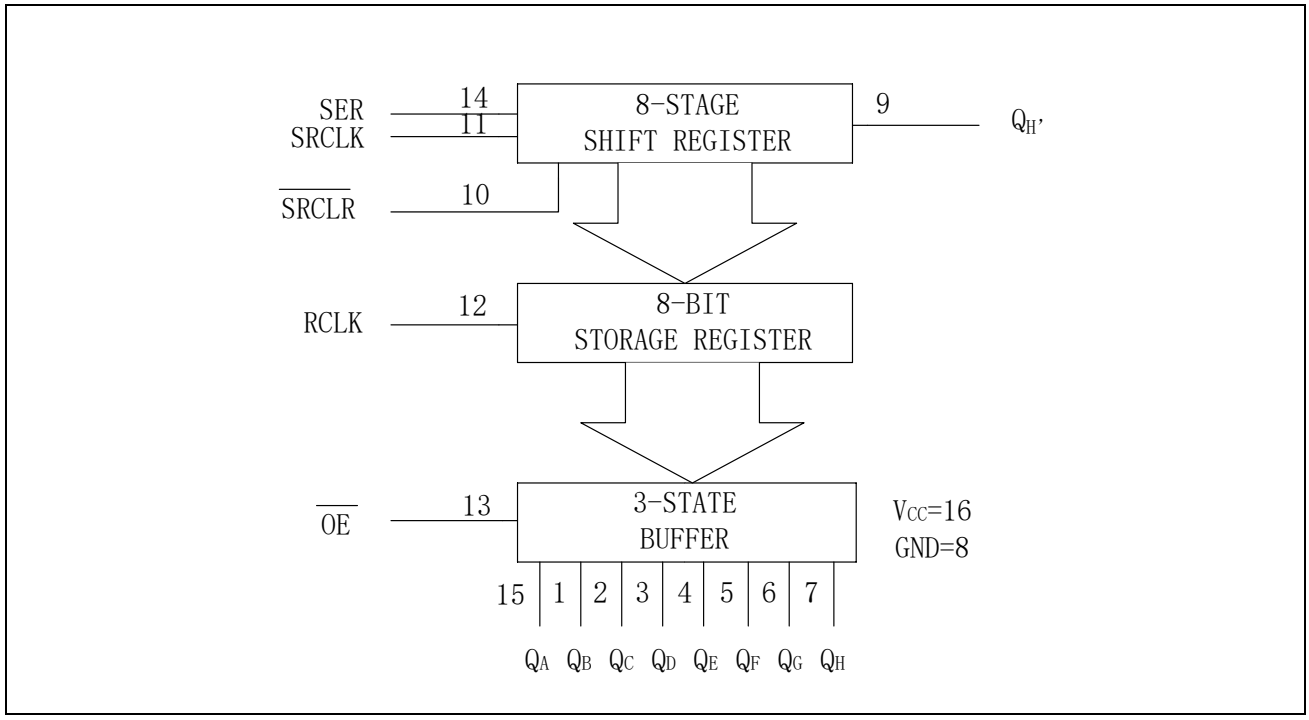


Table 2. Pin description

Pinno	Symbol	Nameandfunction
1, 2, 3, 4, 5, 6, 7, 15	Q_A to Q_H	Data Outputs
9	Q_H'	Serial Data Outputs
10	$\overline{SRCLR}$	Shift Register Clear Input
11	SRCLK	Shift Register Clock Input
13	$\overline{OE}$	Output Enable Input
14	SER	Serial Data Input
12	RCLK	Storage Register Clock Input
8	GND	Ground (0 V)
16	VCC	Positive Supply Voltage

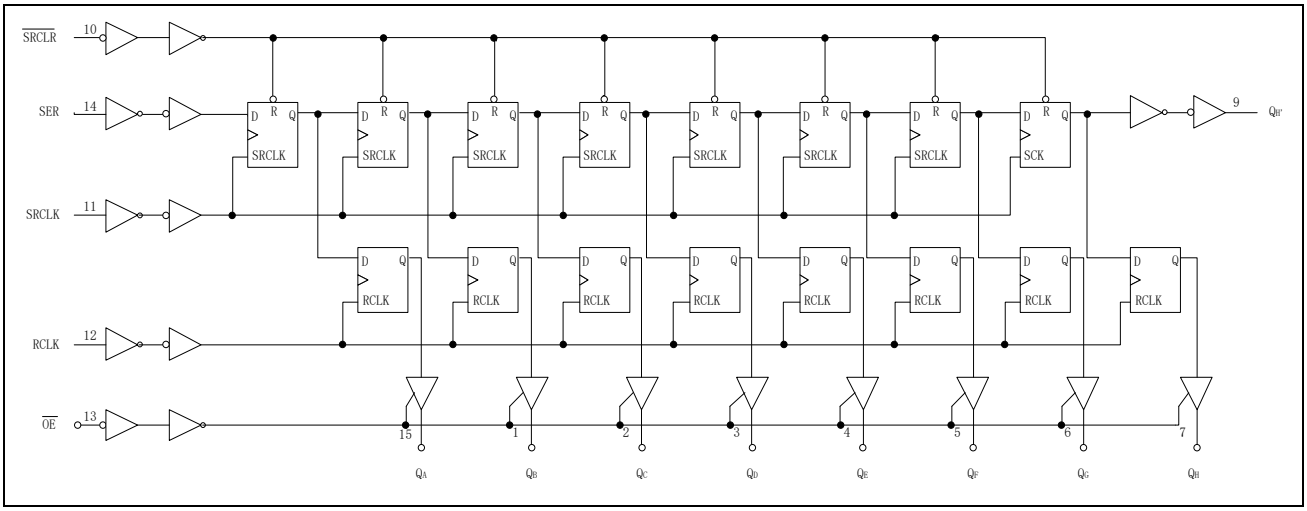
2 Functional description

Figure 2. Block diagram



This block diagram has not be used to estimate propagation delays.

Figure 3. Logic diagram



Thislogicdiagramhasnotbeusedtoestimatepropagationdelays.

Table 3. Truth table(1)

Inputs					Outputs
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Q_A through Q_H outputs disable
X	X	X	X	L	Q_A through Q_H outputs enable
X	X	L	X	X	Shift register is cleared
L	↑	H	X	X	First stage of S.R. becomes “L” other stages store the data of previous stage, respectively
H	↑	H	X	X	First stage of S.R. becomes “H” other stages store the data of previous stage, respectively
X	↓	H	X	X	State of S.R. is not changed
X	X	X	↑	X	S.R. data is stored into storage register
X	X	X	↓	X	Storage register state is not changed

1. X: don’tcare.

Figure 4. Input and output equivalent circuit

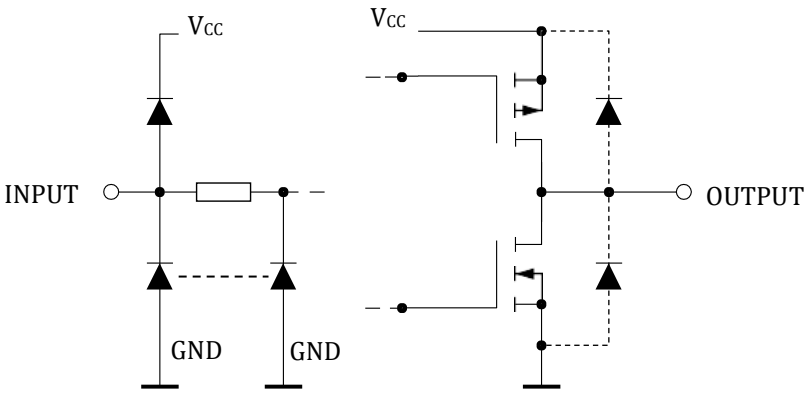
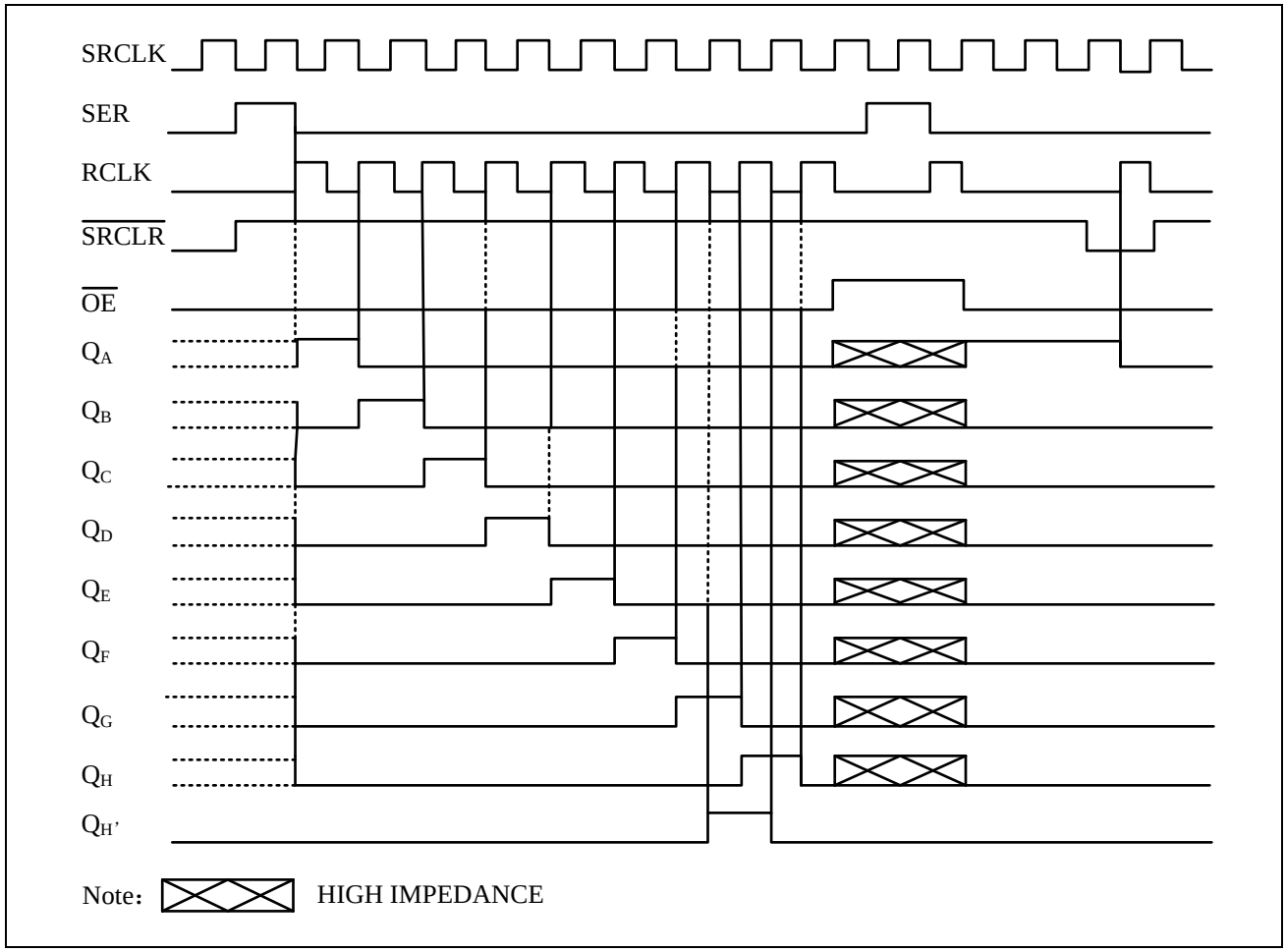


Figure 5. Timing chart



3 Electrical characteristics

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 7.0	V
V_I	DC Input Voltage	-0.5 to V_{CC}+ 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC}+ 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 35	mA
I_{CC}or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500	mW
T_{stg}	Storage Temperature	-65 to + 150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

Table 6. DC specifications

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		V
		4.5		3.15			3.15		
		6.0		4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5	V
		4.5				1.35		1.35	
		6.0				1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20μA	1.9			1.9		V
		4.5	I_O=-20μA	4.4			4.4		
		6.0	I_O=-20μA	5.9			5.9		
		4.5	I_O=-6.0 mA	4.18			4.13		
		6.0	I_O=-7.8 mA	5.68			5.63		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 μA			0.1		0.1	V
		4.5	I_O=20 μA			0.1		0.1	
		6.0	I_O=20 μA			0.1		0.1	
		4.5	I_O=6.0 mA			0.26		0.33	
		6.0	I_O=7.8 mA			0.26		0.33	
I_I	Input Leakage Current	6.0	V_I = V_{CC}or GND			±0.1		±1	μA
I_{OZ}	High Impedance Output Leakage Current	6.0	V_I= V_{IH}orV_{IL} V_I= V_{CC}or GND			±0.5		±5	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40	mA

Table 7. AC electrical characteristics (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	Test Condition			Value					Unit
		V_{CC} (V)	C_L(pF)		T_A= 25°C			-40 to 85°C		
					Min	Typ	Max	Min	Max	
$t_{TLH}t_{THL}$	Output Transition Time (Qn)	2.0	50			25	60		75	ns
		4.5				7	12		15	
		6.0				6	10		13	
$t_{TLH}t_{THL}$	Output Transition Time ($Q_{H'}$)	2.0	50			30	75		95	ns
		4.5				8	15		19	
		6.0				7	13		16	
$t_{PLH}t_{PHL}$	Propagation Delay Time (SRCLK – $Q_{H'}$)	2.0	50			45	125		155	ns
		4.5				15	25		31	
		6.0				13	21		26	
$t_{PLH}t_{PHL}$	Propagation Delay Time ($\overline{SRCLK}$ – $Q_{H'}$)	2.0	50			60	175		220	ns
		4.5				18	35		44	
		6.0				15	30		37	
$t_{PLH}t_{PHL}$	Propagation Delay Time (RCLK – Qn)	2.0	50			60	150		190	ns
		4.5				20	30		38	
		6.0				17	26		32	
		2.0	150			75	190		240	ns
		4.5				25	38		48	
		6.0				22	32		41	
$t_{PZL}t_{PZH}$	High Impedance Output Enable Time	2.0	50	R_L= 1KΩ		45	135		170	ns
		4.5				15	27		34	
		6.0				13	23		29	
		2.0	150	R_L= 1KΩ		60	175		220	ns
		4.5				20	35		44	
		6.0				17	30		37	
$t_{PLZ}t_{PHZ}$	High Impedance Output Disable Time	2.0	50	R_L= 1KΩ		30	150		190	ns
		4.5				15	30		38	
		6.0				14	26		32	

Table 7. AC electrical characteristics (Input $t_r = t_f = 6ns$) (continued)

Symbol	Parameter	Test Condition			Value					Unit
		V_{CC} (V)	C_L(pF)		T_A= 25°C			-40 to 85°C		
					Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	2.0	50		6.0	17		4.8		MHz
		4.5			30	50		24		
		6.0			35	59		28		
		2.0	150		5.2	14		4.2		MHz
		4.5			26	40		21		
		6.0			31	45		25		
$t_{W(H)}$	Minimum Pulse Width (SRCLK-RCLK)	2.0	50			17	75		95	ns
		4.5				6	15		19	
		6.0				6	13		16	
$t_{W(L)}$	MinimumPilse Width ($\overline{SRCLR}$)	2.0	50			20	75		95	ns
		4.5				6	15		19	
		6.0				6	13		16	
t_s	Minimum Setup Time (SER - CCK)	2.0	50			25	50		65	ns
		4.5				5	10		13	
		6.0				4	9		11	
t_s	Minimum Setup Time (SRCLK-RCLK)	2.0	50			35	75		95	ns
		4.5				8	15		19	
		6.0				6	13		16	
t_s	Minimum Setup Time ($\overline{SRCLR}$-RCLK)	2.0	50			40	100		125	ns
		4.5				10	20		25	
		6.0				7	17		21	
t_h	Minimum Hold Time	2.0	50				0		0	ns
		4.5					0		0	
		6.0					0		0	
t_{REM}	Minimum Clear Removal Time	2.0	50			15	50		65	ns
		4.5				3	10		13	
		6.0				3	9		11	

Table 8. Capacitive characteristics

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min.	Max.	
C_{IN}	Input Capacitance	5.0			5	10		10	pF
C_{PD}	Power Dissipation Capacitance(1)	5.0			184				pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation:
   $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

4 Test circuit

Figure 6. Test circuit

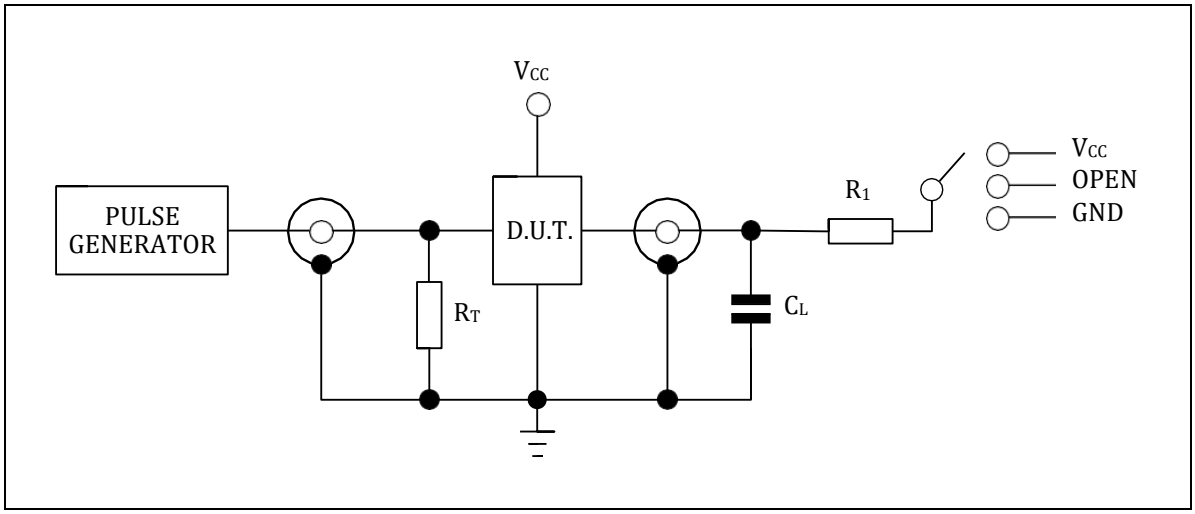


Table9. Propagation delay time configuration

Test	Switch
t_{PLH},t_{PHL}	OPEN
t_{PZL},t_{PLZ}	Vcc
t_{PZH},t_{PHZ}	GND

R_1= 1 KΩ or equivalent
R_T=Z_{OUT} of pulse generator (typically 50 Ω).
C_L = 50 pF/150 pF or equivalent (includes jig and probe capacitance)

Figure 7. Waveform 1: SRCLK to $Q_{H'}$ propagation delay times, SRCLK minimum pulse width (f = 1 MHz; 50 % duty cycle)

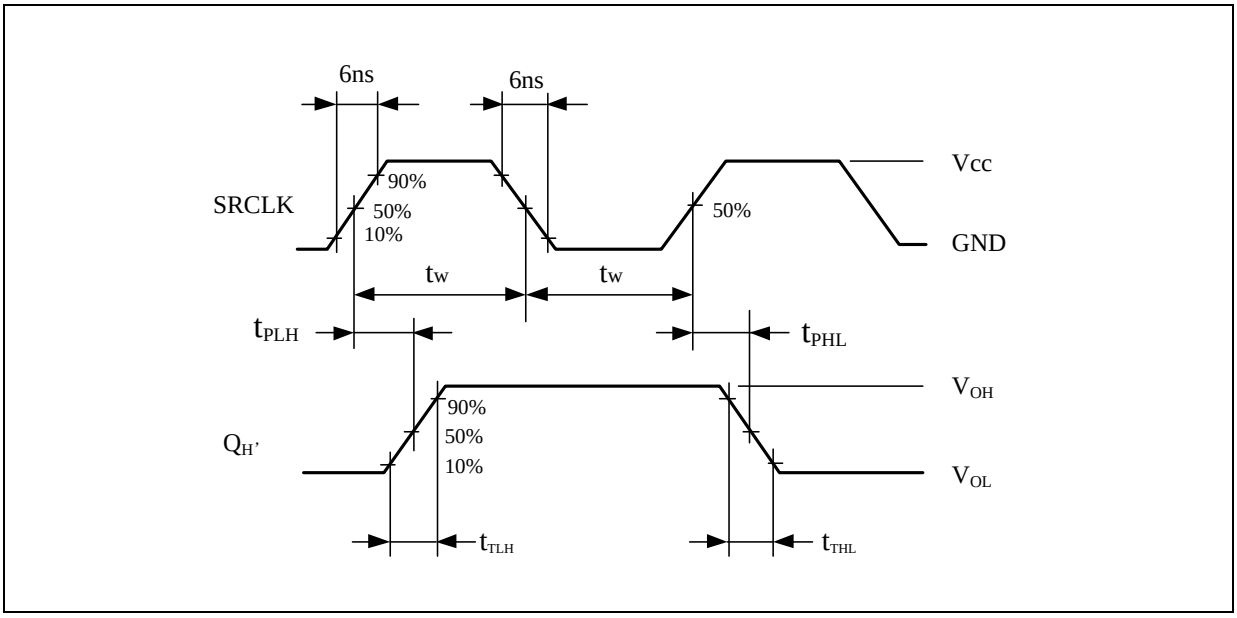


Figure8 . Waveform2 : RCLKto$Q_N$propagationdelaytimes(f=1MHz;50%dutycycle)

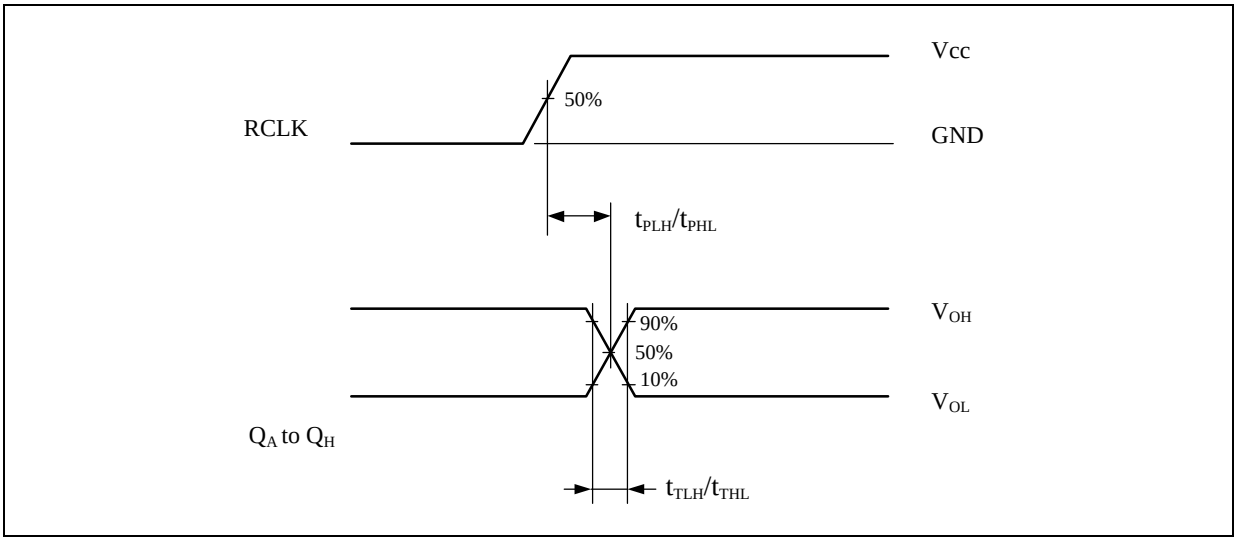


Figure9.Waveform3:SERtoSRCLKsetupandholdtimes(f=1MHz;50%dutycycle)

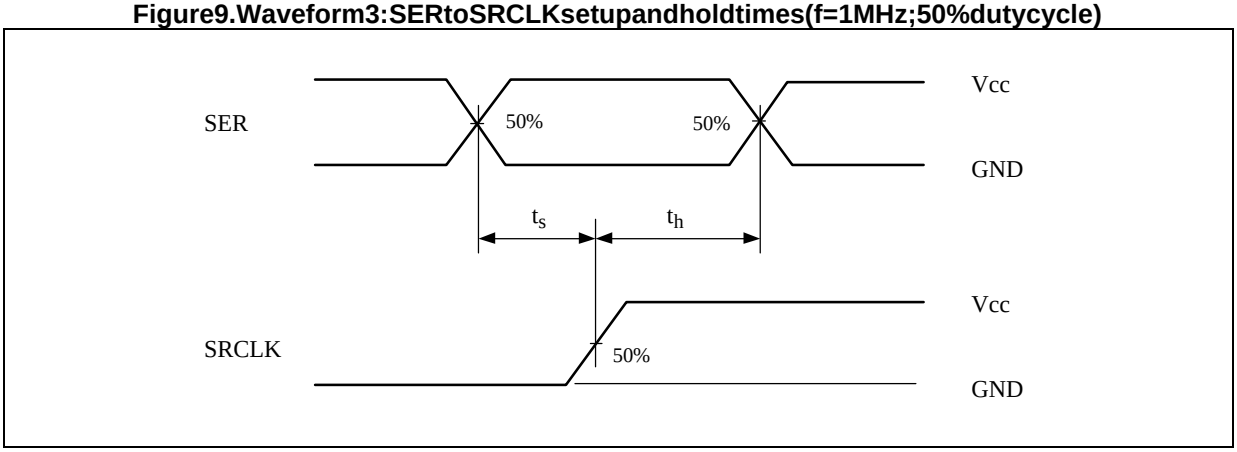


Figure10.Waveform4:SRCLKtoRCLKsetupandholdtimes(f=1MHz;50%dutycycle)

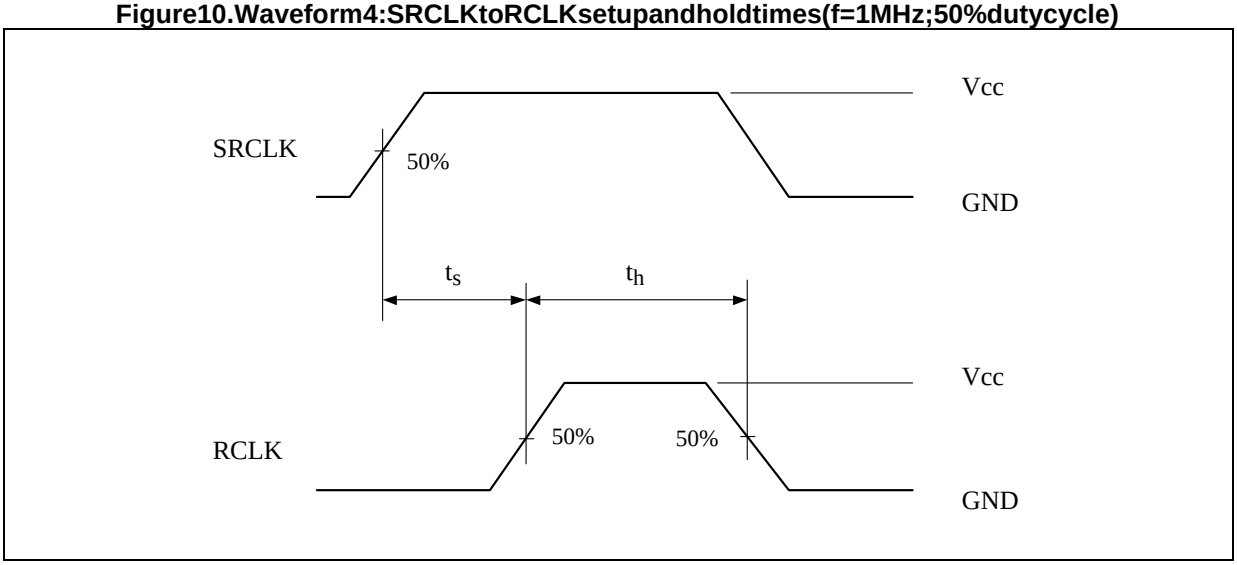


Figure 11. Waveform 5: $\overline{\text{SRCLR}}$ minimum pulse width, minimum removal time (f = 1 MHz; 50 % duty cycle)

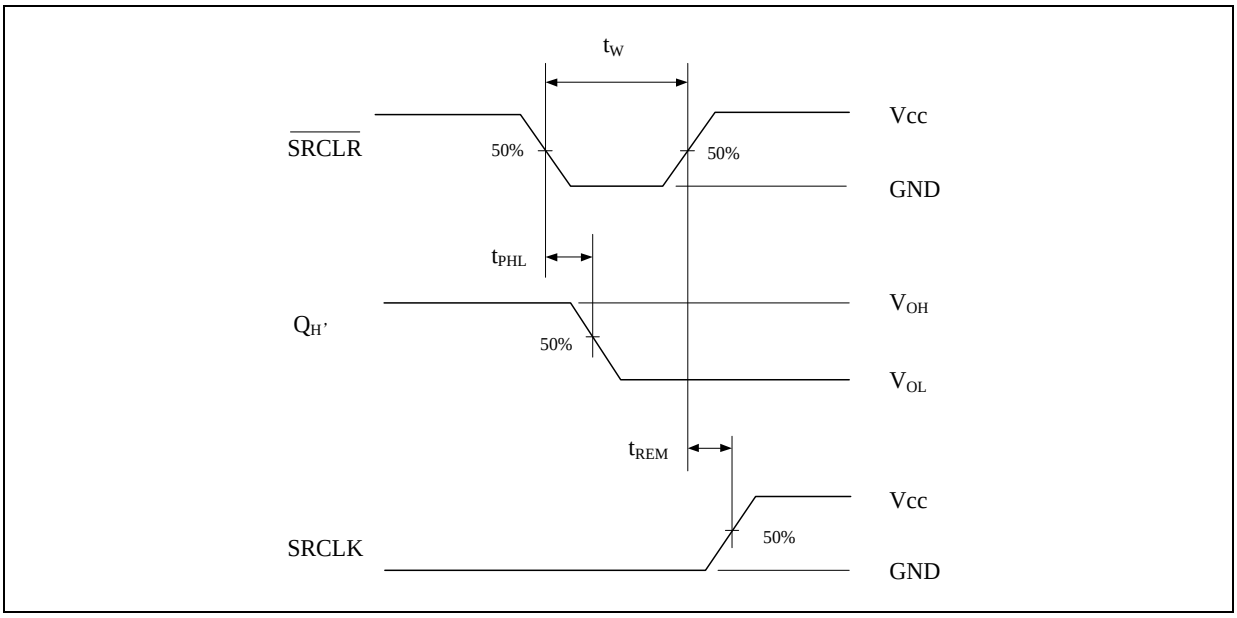


Figure12.Waveform6:Outputenableanddisabletimes(f=1MHz;50%dutycycle)

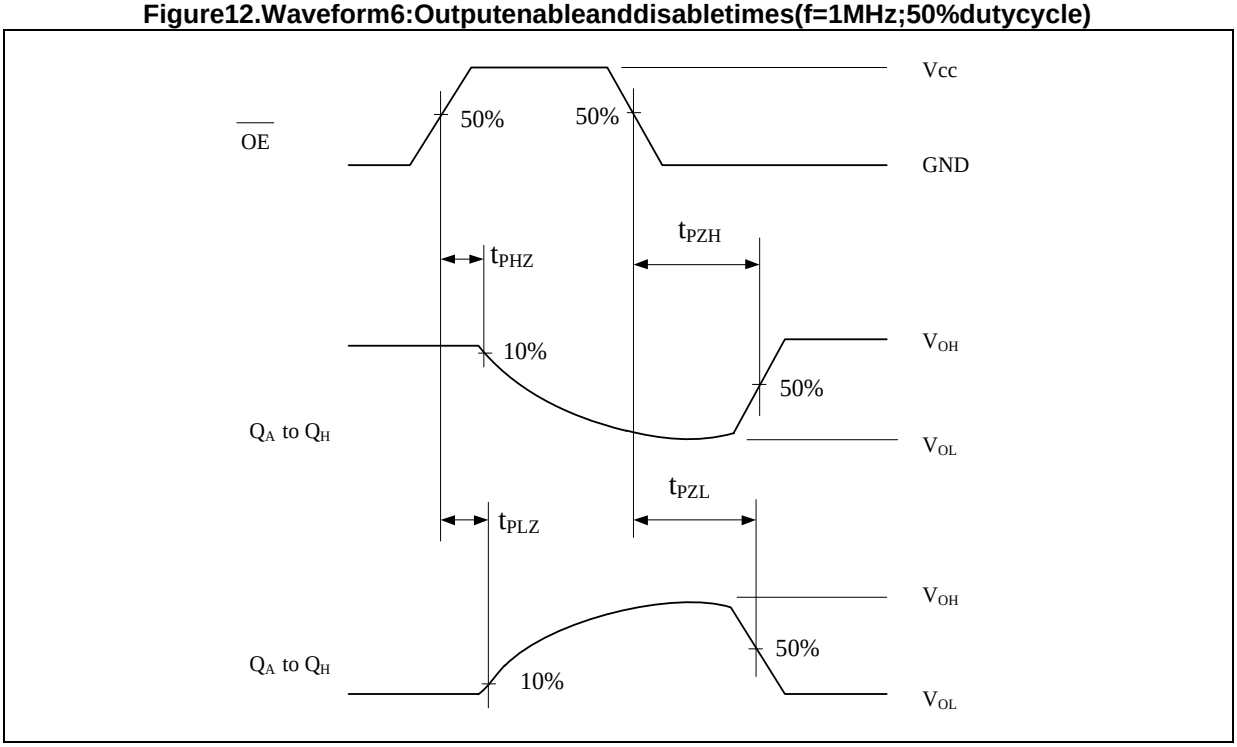
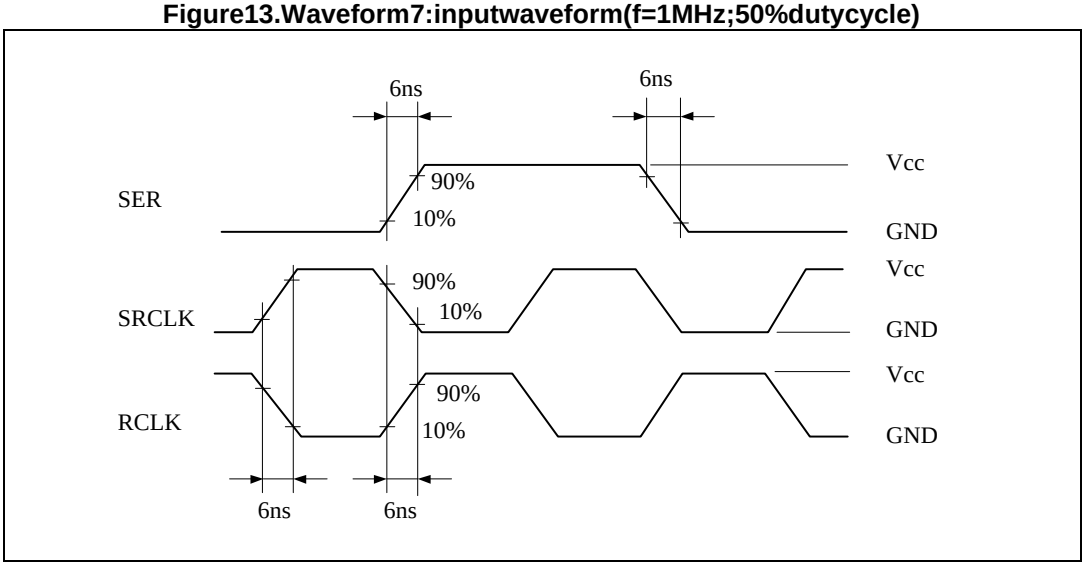
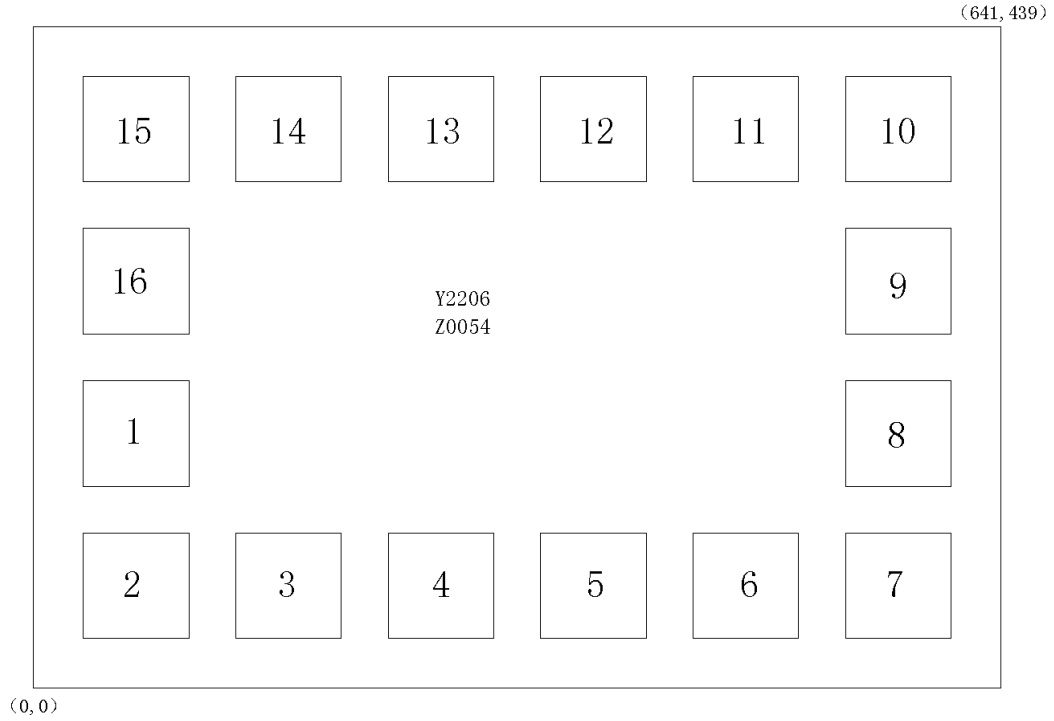


Figure13.Waveform7:inputwaveform(f=1MHz;50%dutycycle)



5 Die Information

Die Type	RD74HC595	Wafer Size	8 Inch
Die Size (μm)	X/Y: 641/439	Bond Area (μm)	X/Y: 70/70
Scribeline (μm)	60	Chip Thickness	
Metal	Front	Al+0.5%Cu	
	Back	Si	
	Top Metal Thickness	9000Å	



Pin No.	Pin Name	Coordinate			Pin No.	Pin Name	Coordinate	
		X	Y				X	Y
1	Q_A	68.0	169.0		9	QH’	573.0	270.0
2	Q_B	68.0	68.0		10	$\overline{SRCLR}$	573.0	371.0
3	Q_C	169.0	68.0		11	SRCLK	472.0	371.0
4	Q_D	270.0	68.0		12	RCLK	371.0	371.0
5	Q_E	371.0	68.0		13	$\overline{OE}$	270.0	371.0
6	Q_F	472.0	68.0		14	SER	169.0	371.0
7	Q_G	573.0	68.0		15	QH	68.0	371.0
8	GND	573.0	169.0		16	V_{CC}	68.0	270.0

6 Ordering information

Table 10. Device summary

Order code	Package	Packing
RD74HC595BDI	DIP16	Tape and reel
RD74HC595BSO	SOP16	
RD74HC595BTS	TSSOP16	
RD74HC595B		Wafer

7 Revision history

Table 11. Document revision history [1]

Date	Revision	Changes
18-Jan-2022	1	Initial release
12-Dec-2023	2	Added : Die information Revised document presentation, minor textual updates

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