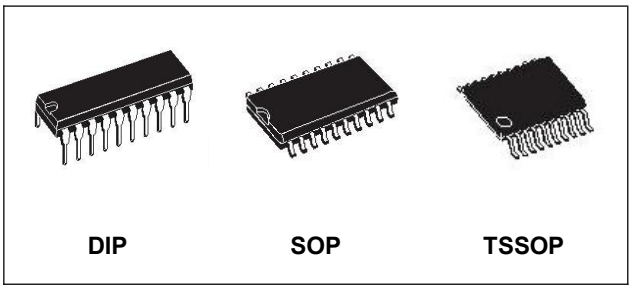
Beijing Relitech Co., LTD.

RD74HC573

OCTAL D-TYPE LATCH WITH 3 STATE OUTPUT NON INVERTING

Datasheet- production data



DIP SOP TSSOP

Features

- HIGH SPEED:
  t_{PD} = 13ns (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 4μA (MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  V_{NIH} = V_{NIL} = 28% V_{CC}(MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}|$ = I_{OL} = 6mA (MIN.)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC}(OPR.) = 2V to 6V

Description

The RD74HC573 is a high-speed CMOS OCTAL LATCH WITH 3-STATE OUTPUTS fabricated with silicon gate CMOS technology.

This 8-BIT D-Type latches is controlled by a latch enable input (LE) and output enable input ($\overline{OE}$).

While the LE input is held at a high level, the Q outputs will follow the data input precisely. When LE is taken low, the Q outputs will be latched precisely at the logic level of D input data.

While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while is at high level the outputs will be in a high impedance state.

The 3-State output configuration and the wide choice of outline make bus organized system simple.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

PART NUMBER	PACKAGE
RD74HC573BDI	DIP20
RD74HC573BSO	SOP20
RD74HC573BTS	TSSOP20

1 Pin information

Figure 1. Pin connection and IEC logic symbols

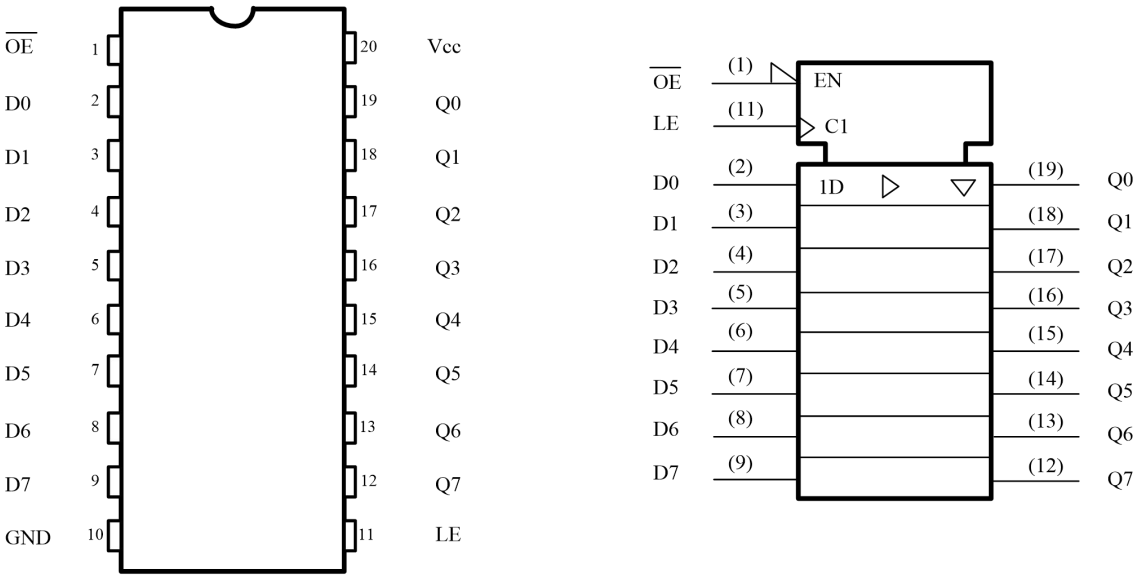


Table 2. Pin description

Pin No	Symbol	Name and function
1	$\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0 to Q7	3 State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

2 Functional description

Figure 2. Logic diagram

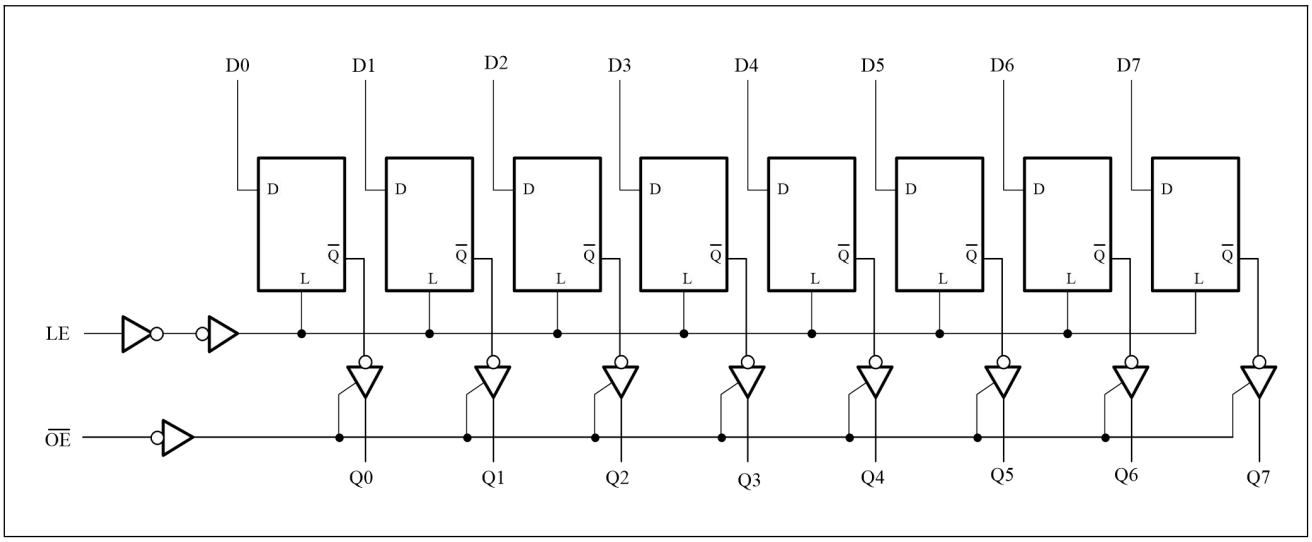
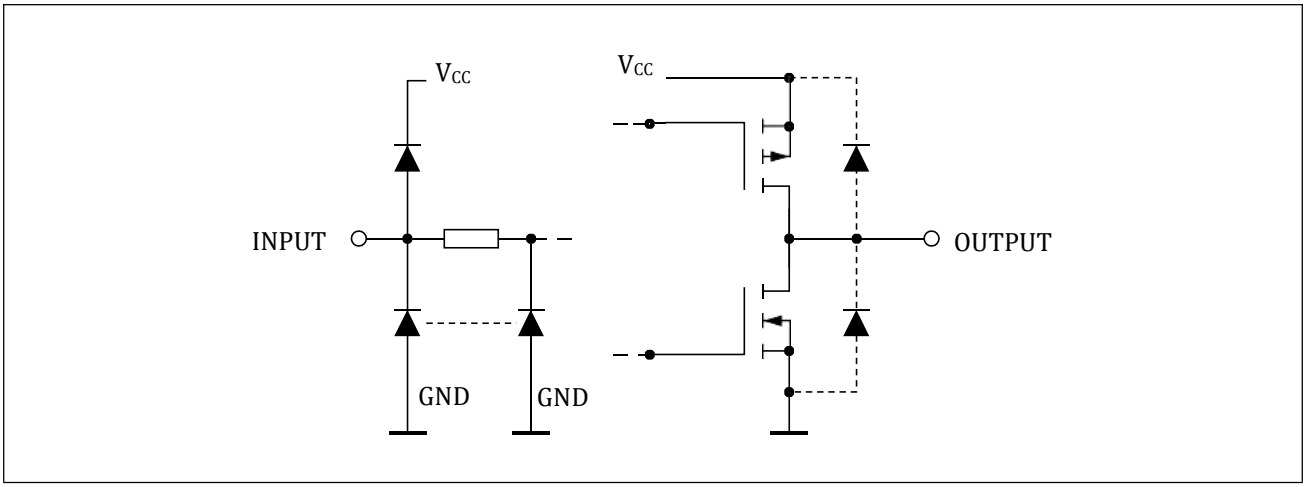


Table 3. Truth table

INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE(*)
L	H	L	L
L	H	H	H

X = Don't care
Z = High impedance
(*): Q Outputs are latched at the time when the LE input is taken low logic level.

Figure 3. Input and output equivalent circuit



3 Electrical characteristics

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 7.0	V
V_I	DC Input Voltage	-0.5 to V_{CC}+ 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC}+ 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 35	mA
I_{CC} or I_{GND}	DC Vcc or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature Range	-65 to + 150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

Table 6. DC specifications

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85°C		
				Min	Typ	Max	Min	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		V
		4.5		3.15			3.15		
		6.0		4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5	V
		4.5				1.35		1.35	
		6.0				1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20μA	1.9	2.0		1.9		V
		4.5	I_O=-20μA	4.4	4.5		4.4		
		6.0	I_O=-20μA	5.9	6.0		5.9		
		4.5	I_O=-6.0 mA	4.18	4.31		4.13		
		6.0	I_O=-7.8 mA	5.68	5.8		5.63		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 μA		0.0	0.1		0.1	V
		4.5	I_O=20 μA		0.0	0.1		0.1	
		6.0	I_O=20 μA		0.0	0.1		0.1	
		4.5	I_O=6.0 mA		0.17	0.26		0.33	
		6.0	I_O=7.8 mA		0.18	0.26		0.33	
I_I	Input Leakage Current	6.0	V_I = V_{CC}or GND			± 0.1		±1	μA
I_{OZ}	High Impedance Output Leakage Current	6.0	V_I = V_{IH} or V_{IL} V_O= V_{CC}or GND			± 0.5		±5	μA
I_{CC}	Quiescent Supply Current	6.0	V_I= V_{CC}or GND			4		40	μA

Table 7. AC electrical characteristics (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	Test Condition			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A= 25°C			-40 to 85°C		
					Min.	Typ.	Max	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75	ns
		4.5				7	12		15	
		6.0				6	10		13	
t_{PLH} t_{PHL}	Propagation Delay Time (LE - Q)	2.0	50			50	115		145	ns
		4.5				15	23		29	
		6.0				13	20		25	
		2.0	150			60	155		195	ns
		4.5				20	31		39	
		6.0				17	26		33	
t_{PLH} t_{PHL}	Propagation Delay Time (D - Q)	2.0	50			42	110		140	ns
		4.5				14	22		28	
		6.0				12	19		24	
		2.0	150			57	150		190	ns
		4.5				19	30		38	
		6.0				16	26		32	
t_{PZL} t_{PZH}	High Impedance Output Enable Time	2.0	50	R_L = 1 KΩ		55	140		175	ns
		4.5				17	28		35	
		6.0				14	24		30	
		2.0	150	R_L = 1 KΩ		66	180		225	ns
		4.5				22	36		45	
		6.0				19	31		38	
t_{PLZ} t_{PHZ}	High Impedance Output Disable Time	2.0	50	R_L = 1 KΩ		40	125		155	ns
		4.5				17	25		31	
		6.0				15	21		26	
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width	2.0	50			40	75		95	ns
		4.5				8	15		19	
		6.0				7	13		16	
t_s	Minimum Set-up Time	2.0	50			16	50		65	ns
		4.5				5	10		13	
		6.0				3	9		11	
t_h	Minimum Hold Time	2.0	50				5		5	ns
		4.5					5		5	
		6.0					5		5	

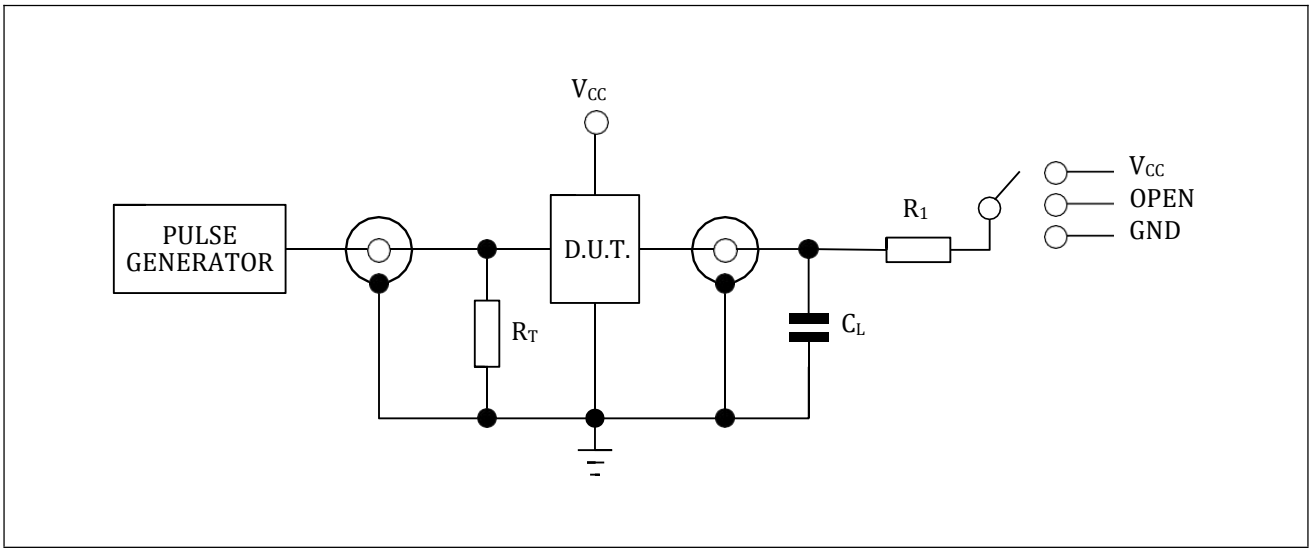
Table 8. Capacitive characteristics

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min.	Max.	
C_{IN}	Input Capacitance				5	10		10	pF
C_{OUT}	Output Capacitance				10				pF
C_{PD}	Power Dissipation Capacitance(1)				51				pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per Flip Flop) and the C_{PD} when n pcs of Flip Flop operate, can be gained by the following equation: $C_{PD(TOTAL)} = 33 + 18 \times n(pF)$

4 Test circuit

Figure 4. Test circuit



TEST	SWITCH
t_{PLH}, t_{PHL}	OPEN
t_{PZL}, t_{PLZ}	VCC
t_{PZH}, t_{PHZ}	GND

R_T = Z_{OUT} of pulse generator (typically 50Ω)
R_1 = 1KΩ or equivalent
C_L = 50pF/150pF or equivalent (includes jig and probe capacitance)

Figure 5. Waveform 1: LE to Qn propagation delays, LE minimum pulse width, Dn to LE setup and hold time (f=1MHz; 50% duty cycle)

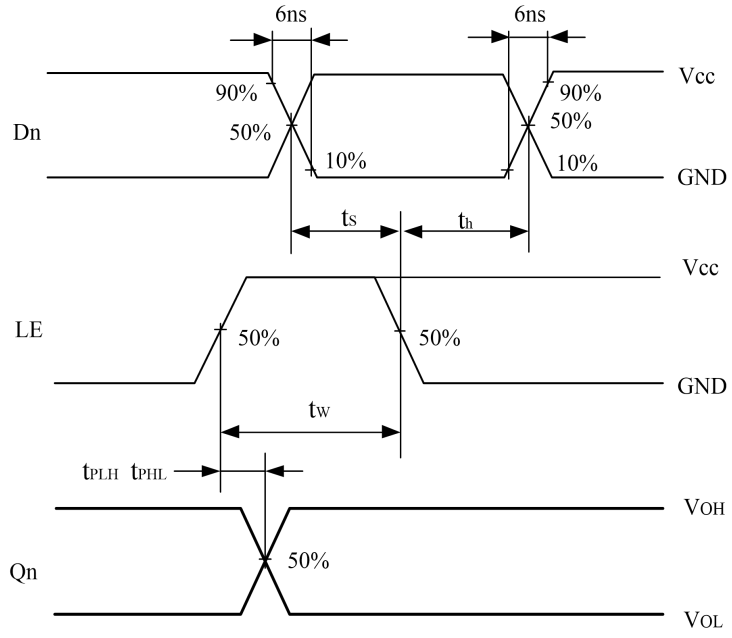


Figure 6. Waveform 2: output enable and disable times (f= 1MHz; 50% duty cycle)

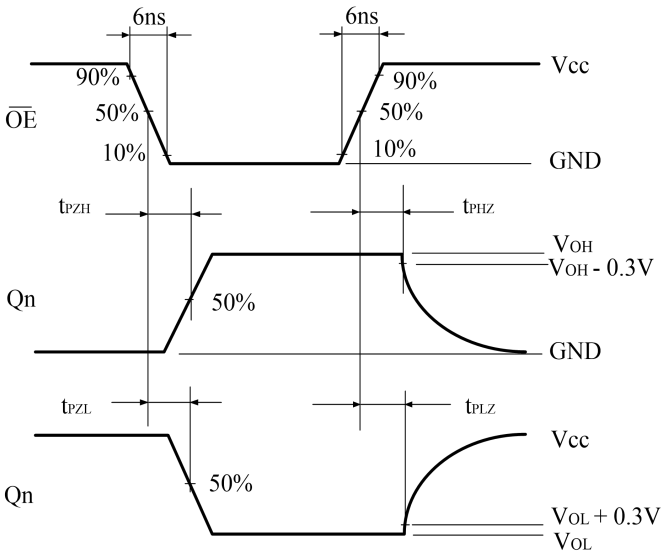
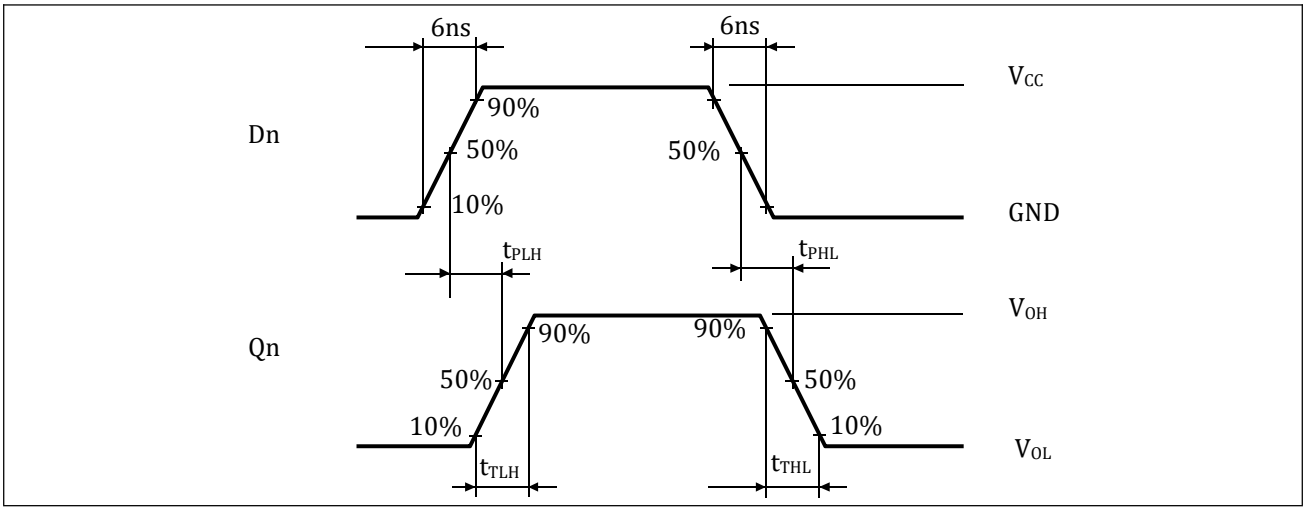
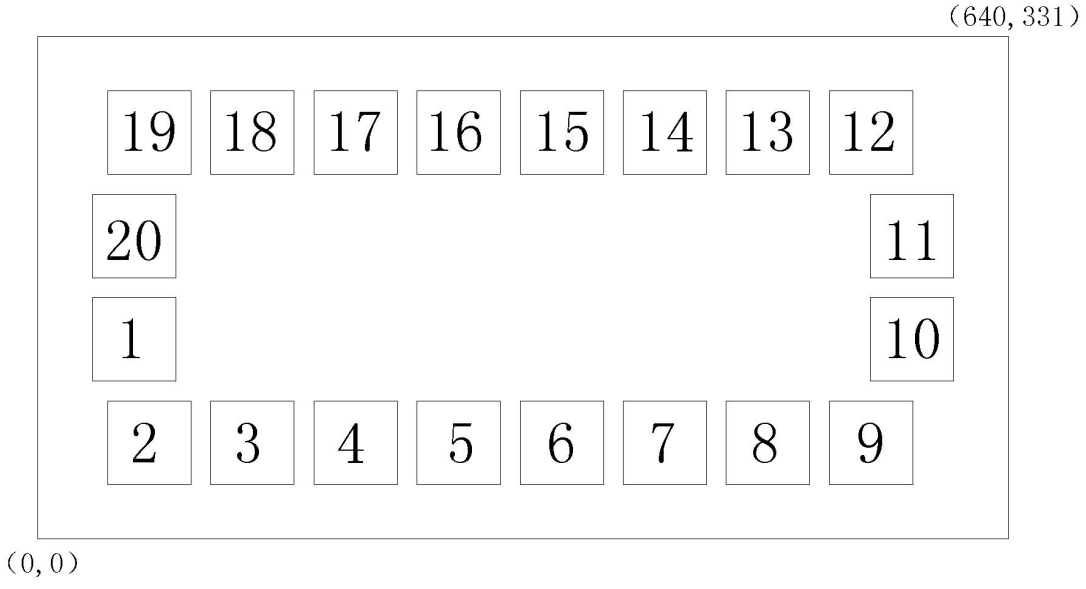


Figure 7. Waveform 3: propagation delay time (f=1MHz; 50% duty cycle)



5 Die Information

Die Type	RD74HC573	Wafer Size	8 Inch
Die Size (μm)	X/Y: 657/331	Bond Area (μm)	X/Y: 55/55
Scribeline (μm)	60	Chip Thickness	
Metal	Front	Al+0.5%Cu	
	Back	Si	
	Top Metal Thickness	9000Å	



Pin No.	Pin Name	Coordinate			Pin No.	Pin Name	Coordinate	
		X	Y				X	Y
1	$\overline{OE}$	63.5	131.5		11	LE	576.5	199.5
2	D0	73.5	63.5		12	Q7	549.5	267.5
3	D1	141.5	63.5		13	Q6	481.5	267.5
4	D2	209.5	63.5		14	Q5	413.5	267.5
5	D3	277.5	63.5		15	Q4	345.5	267.5
6	D4	345.5	63.5		16	Q3	277.5	267.5
7	D5	413.5	63.5		17	Q2	209.5	267.5
8	D6	481.5	63.5		18	Q1	141.5	267.5
9	D7	549.5	63.5		19	Q0	73.5	267.5
10	GND	576.5	131.5		20	V_{CC}	63.5	199.5

6 Ordering information

Table 9. Device summary

Order code	Package	Packing
RD74HC573BDI	DIP20	Tape and reel
RD74HC573BSO	SOP20	
RD74HC573BTS	TSSOP20	
RD74HC573B		Wafer

7 Revision history

Table 10. Document revision history (1)

Date	Revision	Changes
18-Jan-2022	1	Initial release
12-Dec-2023	2	Added : Die information Revised document presentation, minor textual updates

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