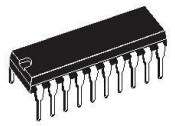
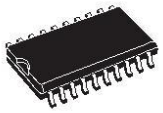
Beijing Relitech Co., LTD.

# RD74HC374

## OCTAL D-TYPE FLIP FLOP WITH 3 STATE OUTPUT NON INVERTING

**Datasheet- production data**


**DIP** **SOP** **TSSOP**

## Features

- HIGH SPEED:
  $f_{MAX}$ = 90MHz (TYP.) at $V_{CC}$ = 6V
- LOW POWER DISSIPATION:
  $I_{CC}$ = 4μA (MAX.) at $T_A$=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH}$ = $V_{NIL}$ = 28% $V_{CC}$(MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}|$ = $I_{OL}$ = 6mA (MIN.)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  $V_{CC}$(OPR) = 2V to 6V

## Description

The RD74HC374 is a high-speed CMOS OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUTS NON-INVERTING fabricated with sub-micron silicon gate CMOS technology.

This 8-bit D-TYPE FLIP FLOP is controlled by a clock input (CK) and an output enable input ($\overline{OE}$). On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs.

While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while $\overline{OE}$ is high the outputs will be in a high impedance state.

The output control does not affect the internal operation of flip-flops; that is, the old data can be retained or the new data can be entered even while the outputs are off.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

**Table 1. Device summary**

| PART NUMBER | PACKAGE |
|---|---|
| RD74HC374BDI | DIP20 |
| RD74HC374BSO | SOP20 |
| RD74HC374BTS | TSSOP20 |

# 1 Pin information

**Figure 1. Pin connection and IEC logic symbols**

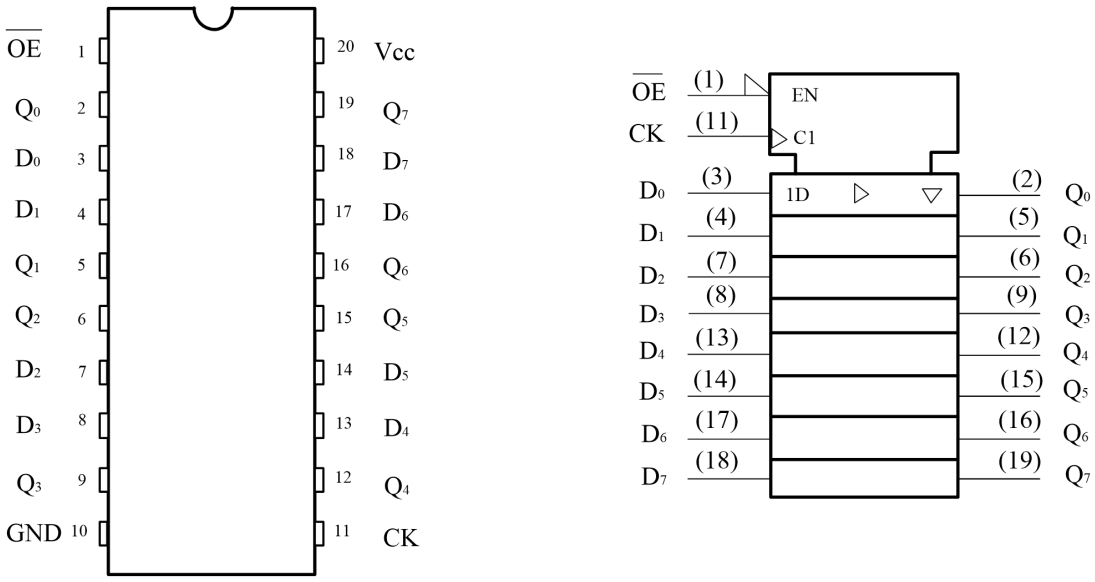



**Table 2. Pin description**

| Pin No | Symbol | Name and function |
|---|---|---|
| 1 | $\overline{OE}$ | 3 State Output Enable Input (Active LOW) |
| 2, 5, 6, 9, 12, 15, 16, 19 | Q0 to Q7 | 3 State Outputs |
| 3, 4, 7, 8, 13, 14, 17, 18 | D0 to D7 | Data Inputs |
| 11 | CK | Clock Input (LOW to HIGH, Edge Triggered) |
| 10 | GND | Ground (0V) |
| 20 | $V_{CC}$ | Positive Supply Voltage |

# 2 Functional description

**Table 3. Truth table**

| INPUTS | | | OUTPUTS |
|---|---|---|---|
| $\overline{OE}$ | CK | D | Q |
| H | X | X | Z |
| L | ⌝⌞ | X | NO CHANGE |
| L | ⌞⌜ | L | L |
| L | ⌞⌜ | H | H |

X = Don't care
Z = High impedance

**Figure 2. Input and output equivalent circuit**

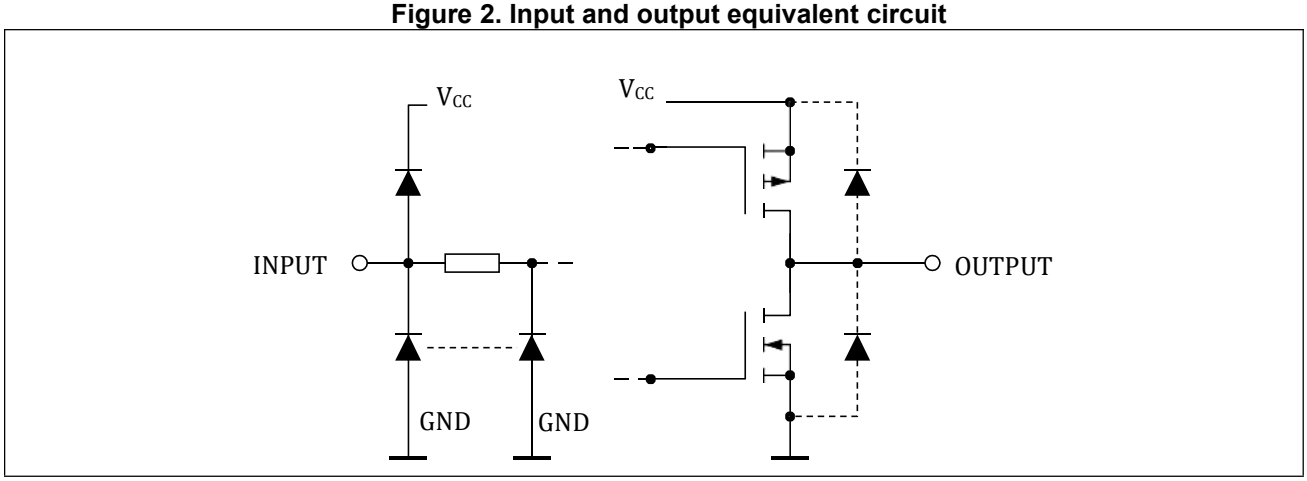
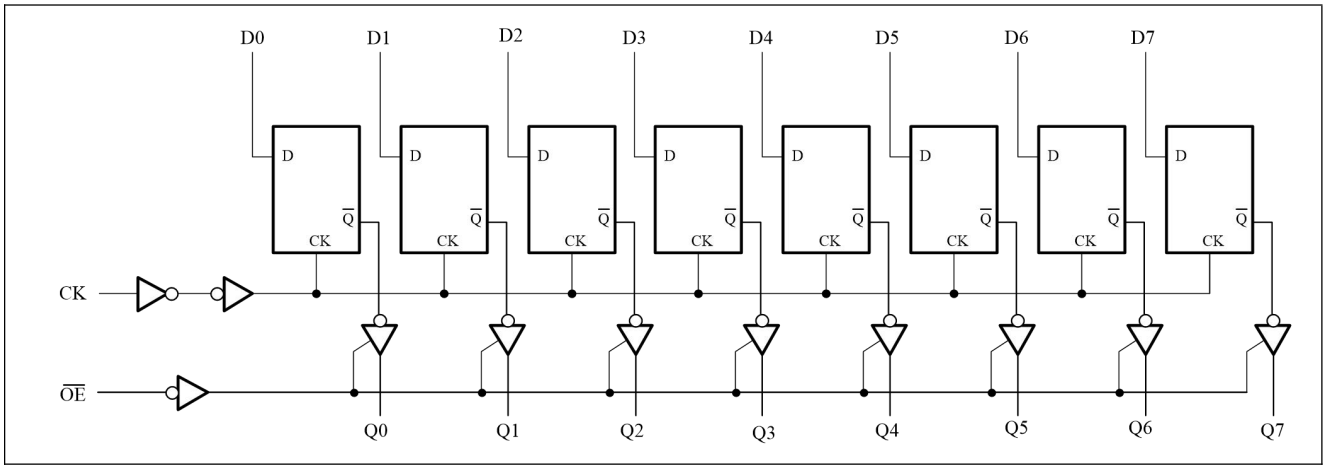



**Figure 3. Logic diagram**




This logic diagram has not be used to estimate propagation delays

# 3 Electrical characteristics

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.5 to + 7.0 | V |
| $V_I$ | DC Input Voltage | -0.5 to $V_{CC}$+ 0.5 | V |
| $V_O$ | DC Output Voltage | -0.5 to $V_{CC}$+ 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | ± 20 | mA |
| $I_{OK}$ | DC Output Diode Current | ± 20 | mA |
| $I_O$ | DC Output Current | ± 35 | mA |
| $I_{CC}$ or $I_{GND}$ | DC VCC or Ground Current | ± 70 | mA |
| $P_D$ | Power Dissipation | 500 (*) | mW |
| $T_{stg}$ | Storage Temperature | -65 to + 150 | °C |
| $T_L$ | Lead Temperature (10 sec) | 300 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

**Table 5. Recommended operating conditions**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 2 to 6 | V |
| $V_I$ | Input Voltage | | 0 to $V_{CC}$ | V |
| $V_O$ | Output Voltage | | 0 to $V_{CC}$ | V |
| $T_{op}$ | Operating Temperature | | -40 to +85 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time | $V_{CC}$ = 2.0V | 0 to 1000 | ns |
| | | $V_{CC}$ = 4.5V | 0 to 500 | ns |
| | | $V_{CC}$ = 6.0V | 0 to 400 | ns |

**Table 6. DC specifications**

| Symbol | Parameter | Test Condition | | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25 °C | | | -40 to 85°C | | |
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | High Level Input Voltage | 2.0 | | 1.5 | | | 1.5 | | V |
| | | 4.5 | | 3.15 | | | 3.15 | | |
| | | 6.0 | | 4.2 | | | 4.2 | | |
| $V_{IL}$ | Low Level Input Voltage | 2.0 | | | | 0.5 | | 0.5 | V |
| | | 4.5 | | | | 1.35 | | 1.35 | |
| | | 6.0 | | | | 1.8 | | 1.8 | |
| $V_{OH}$ | High Level Output Voltage | 2.0 | $I_O$=-20μA | 1.9 | 2.0 | | 1.9 | | V |
| | | 4.5 | $I_O$=-20μA | 4.4 | 4.5 | | 4.4 | | |
| | | 6.0 | $I_O$=-20μA | 5.9 | 6.0 | | 5.9 | | |
| | | 4.5 | $I_O$=-6.0 mA | 4.18 | 4.31 | | 4.13 | | |
| | | 6.0 | $I_O$=-7.8 mA | 5.68 | 5.8 | | 5.63 | | |
| $V_{OL}$ | Low Level Output Voltage | 2.0 | $I_O$=20 μA | | 0.0 | 0.1 | | 0.1 | V |
| | | 4.5 | $I_O$=20 μA | | 0.0 | 0.1 | | 0.1 | |
| | | 6.0 | $I_O$=20 μA | | 0.0 | 0.1 | | 0.1 | |
| | | 4.5 | $I_O$=6.0 mA | | 0.17 | 0.26 | | 0.33 | |
| | | 6.0 | $I_O$=7.8 mA | | 0.18 | 0.26 | | 0.33 | |
| $I_I$ | Input Leakage Current | 6.0 | $V_I$ = $V_{CC}$or GND | | | ±0.1 | | ±1 | μA |
| $I_{OZ}$ | High Impedance Output Leakage Current | 6.0 | $V_I$ = $V_{IH}$ or $V_{IL}$<br>$V_O$= $V_{CC}$or GND | | | ±0.5 | | ±5 | μA |
| $I_{CC}$ | Quiescent Supply Current | 6.0 | $V_I$= $V_{CC}$or GND | | | 4 | | 40 | μA |

**Table 7. AC electrical characteristics ($C_L$ = 50pF, Input $t_r$ = $t_f$ = 6ns)**

| Symbol | Parameter | Test Condition | | | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | $C_L$ (pF) | | $T_A$= 25°C | | | -40 to 85°C | | |
| | | | | | Min | Typ | Max | Min | Max | |
| $t_{TLH}$ $t_{THL}$ | Output Transition Time | 2.0 | 50 | | | 25 | 60 | | 75 | ns |
| | | 4.5 | | | | 7 | 12 | | 15 | |
| | | 6.0 | | | | 6 | 10 | | 13 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (CLOCK – Q) | 2.0 | 50 | | | 45 | 140 | | 175 | ns |
| | | 4.5 | | | | 15 | 28 | | 35 | |
| | | 6.0 | | | | 13 | 24 | | 30 | |
| | | 2.0 | 150 | | | 60 | 190 | | 240 | ns |
| | | 4.5 | | | | 20 | 38 | | 48 | |
| | | 6.0 | | | | 17 | 32 | | 41 | |
| $t_{PZL}$ $t_{PZH}$ | High Impedance Output Enable Time | 2.0 | 50 | $R_L$ = 1 KΩ | | 39 | 135 | | 170 | ns |
| | | 4.5 | | | | 13 | 27 | | 34 | |
| | | 6.0 | | | | 11 | 23 | | 29 | |
| | | 2.0 | 150 | $R_L$ = 1 KΩ | | 54 | 185 | | 230 | ns |
| | | 4.5 | | | | 18 | 37 | | 46 | |
| | | 6.0 | | | | 15 | 31 | | 39 | |
| $t_{PLZ}$ $t_{PHZ}$ | High Impedance Output Disable Time | 2.0 | 50 | $R_L$ = 1 KΩ | | 30 | 125 | | 155 | ns |
| | | 4.5 | | | | 14 | 25 | | 31 | |
| | | 6.0 | | | | 13 | 21 | | 26 | |
| $f_{MAX}$ | Maximum Clock Frequency | 2.0 | 50 | | 6.2 | 18 | | 5 | | MHz |
| | | 4.5 | | | 31 | 75 | | 25 | | |
| | | 6.0 | | | 37 | 90 | | 30 | | |
| $t_{W(L)}$ $t_{W(H)}$ | Minimum Pulse Width(CLOCK) | 2.0 | 50 | | | 15 | 75 | | 95 | ns |
| | | 4.5 | | | | 6 | 15 | | 19 | |
| | | 6.0 | | | | 6 | 13 | | 16 | |
| $t_s$ | Minimum Set-up Time | 2.0 | 50 | | | 25 | 75 | | 95 | ns |
| | | 4.5 | | | | 6 | 15 | | 19 | |
| | | 6.0 | | | | 4 | 13 | | 16 | |
| $t_h$ | Minimum Hold Time | 2.0 | 50 | | | | 0 | | 0 | ns |
| | | 4.5 | | | | | 0 | | 0 | |
| | | 6.0 | | | | | 0 | | 0 | |

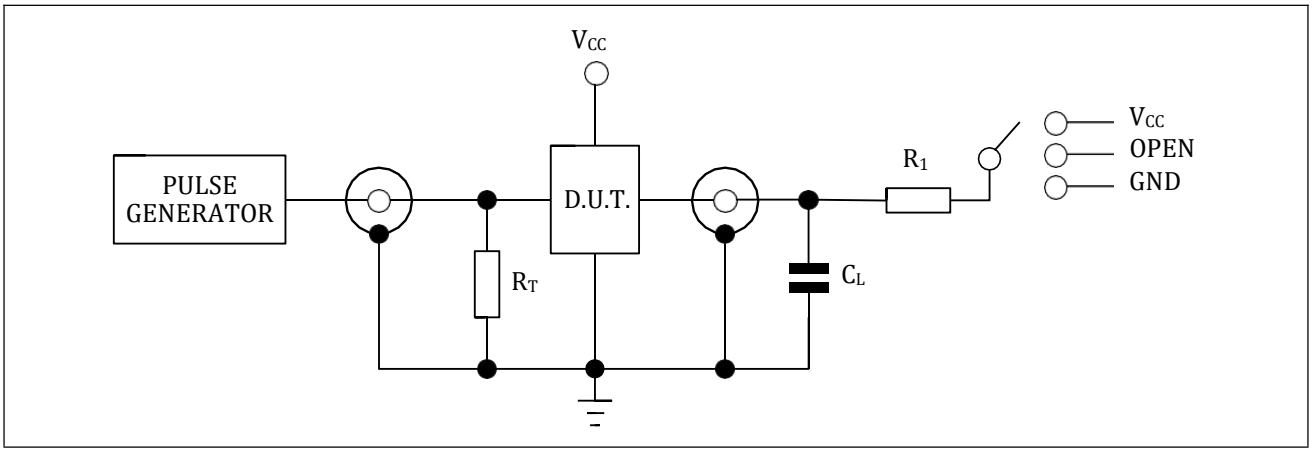
**Table 8. Capacitive characteristics**

| Symbol | Parameter | Test Condition | | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25°C | | | -40 to 85°C | | |
| | | | | Min | Typ | Max | Min | Max | |
| $C_{IN}$ | Input Capacitance | 5.0 | | | 5 | 10 | | 10 | pF |
| $C_{OUT}$ | Output Capacitance | 5.0 | | | 10 | | | | pF |
| $C_{PD}$ | Power Dissipation Capacitance(1) | 5.0 | | | 47 | | | | pF |

1. $C_{PD}$ is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per Flip Flop) and the $C_{PD}$ when n pcs of Flip Flop operate, can be gained by the following equation: $C_{PD(TOTAL)} = 30 + 17 \times n$ (pF)

# 4 Test circuit

**Figure 4. Test circuit**




| TEST | SWITCH |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | OPEN |
| $t_{PZL}$, $t_{PLZ}$ | VCC |
| $t_{PZH}$, $t_{PHZ}$ | GND |

$R_T$ = $Z_{OUT}$ of pulse generator (typically 50Ω)
$R_1$ = 1KΩ or equivalent
$C_L$ = 50pF/150pF or equivalent (includes jig and probe capacitance)

**Figure 5. Waveform 1: CK to Qn propagation delays, CK $f_{MAX}$, Dn to CK setup and hold time (f=1MHz; 50% duty cycle)**

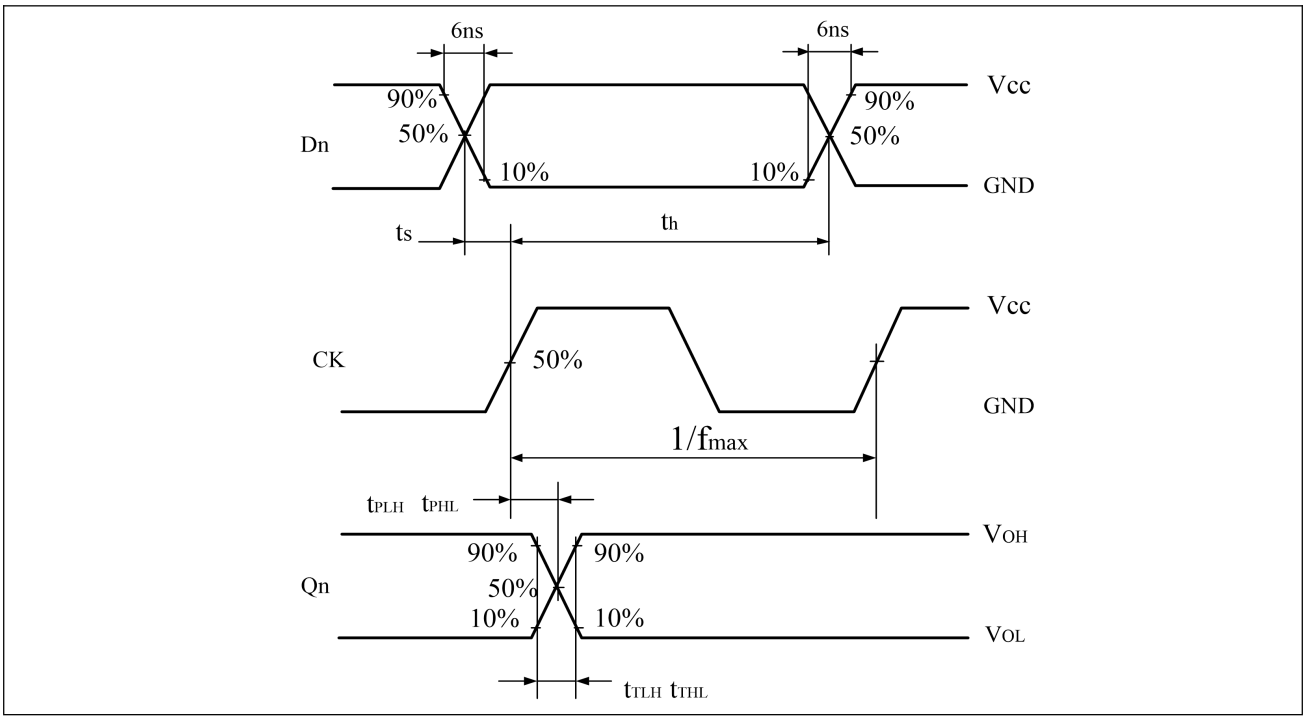



**Figure 6. Waveform 2: output enable and disable times (f= 1MHz; 50% duty cycle)**

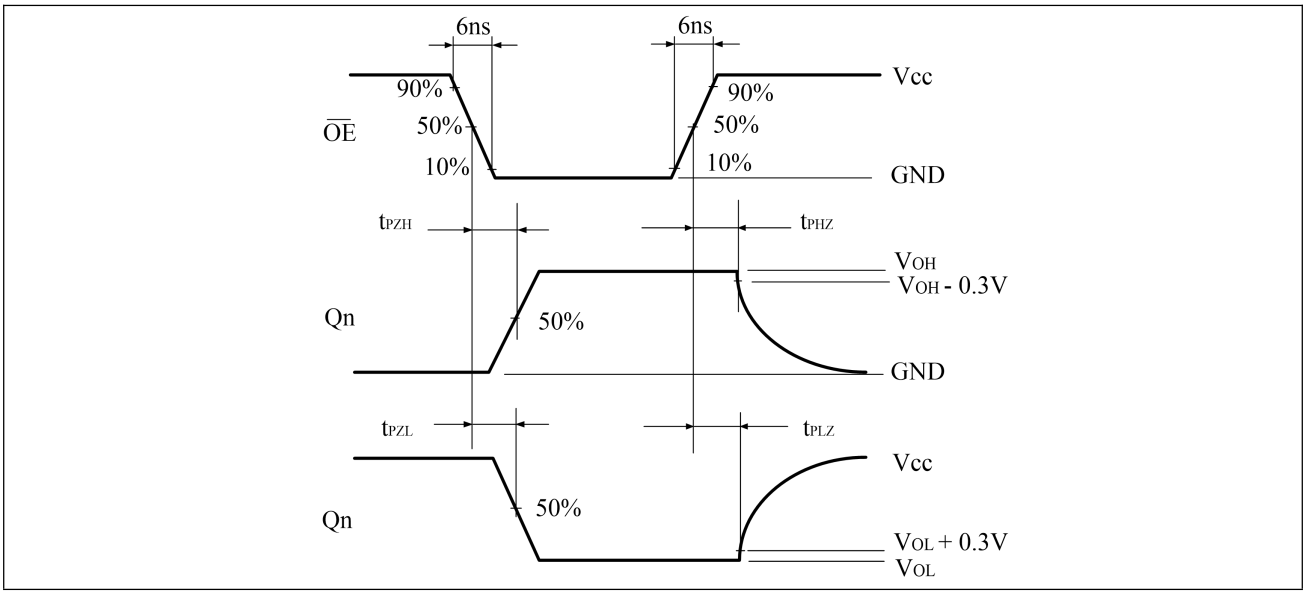
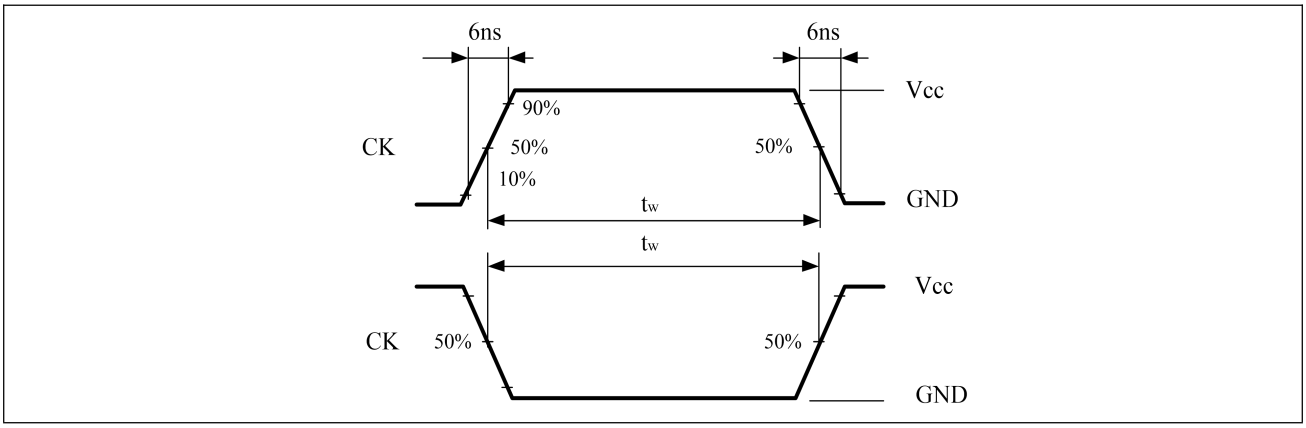
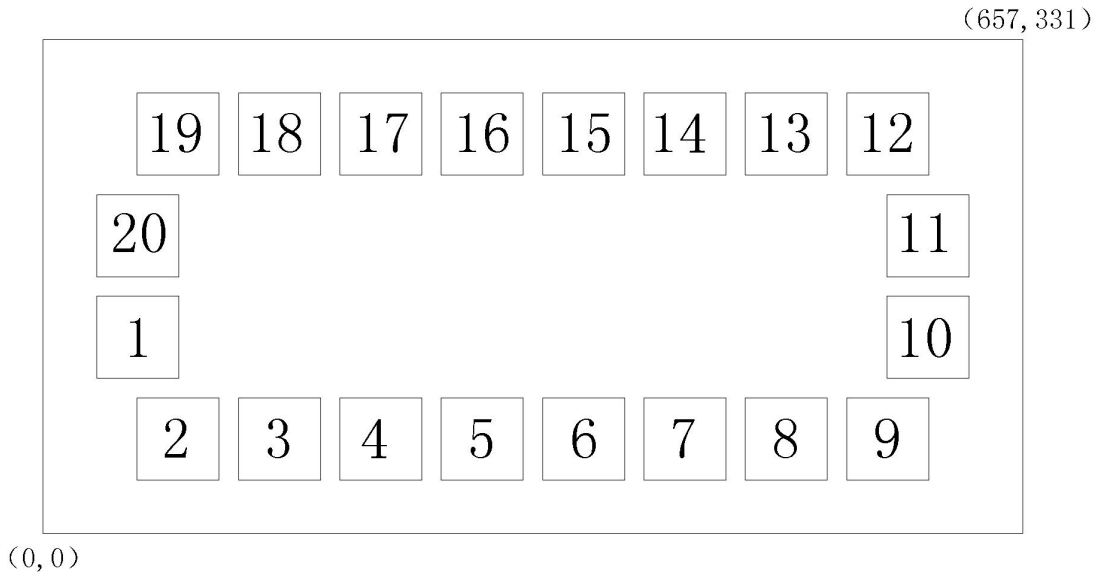


**Figure 7. Waveform 3: minimum pulse width (CK) (f= 1MHz; 50% duty cycle)**




# 5 Die Information

| | | | |
|---|---|---|---|
| Die Type | RD74HC374 | Wafer Size | 8 Inch |
| Die Size (μm) | X/Y: 657/331 | Bond Area (μm) | X/Y: 55/55 |
| Scribeline (μm) | 60 | Chip Thickness | |
| Metal | Front | Al+0.5%Cu | |
| | Back | Si | |
| | Top Metal Thickness | 9000Å | |



| Pin No. | Pin Name | Coordinate | | Pin No. | Pin Name | Coordinate | |
|---|---|---|---|---|---|---|---|
| | | X | Y | | | X | Y |
| 1 | $\overline{OE}$ | 63.5 | 131.5 | 11 | CK | 593.5 | 199.5 |
| 2 | Q0 | 90.5 | 63.5 | 12 | Q4 | 566.5 | 267.5 |
| 3 | D0 | 158.5 | 63.5 | 13 | D4 | 498.5 | 267.5 |
| 4 | D1 | 226.5 | 63.5 | 14 | D5 | 430.5 | 267.5 |
| 5 | Q1 | 294.5 | 63.5 | 15 | Q5 | 362.5 | 267.5 |
| 6 | Q2 | 362.5 | 63.5 | 16 | Q6 | 294.5 | 267.5 |
| 7 | D2 | 430.5 | 63.5 | 17 | D6 | 226.5 | 267.5 |
| 8 | D3 | 498.5 | 63.5 | 18 | D7 | 158.5 | 267.5 |
| 9 | Q3 | 566.5 | 63.5 | 19 | Q7 | 90.5 | 267.5 |
| 10 | GND | 593.5 | 131.5 | 20 | $V_{CC}$ | 63.5 | 199.5 |

# 6 Ordering information

**Table 9. Device summary**

| Order code | Package | Packing |
|---|---|---|
| RD74HC374BDI | DIP20 | Tape and reel |
| RD74HC374BSO | SOP20 | |
| RD74HC374BTS | TSSOP20 | |
| RD74HC374B | | Wafer |

# 7 Revision history

**Table 10. Document revision history [1]**

| Date | Revision | Changes |
|---|---|---|
| 18-Jan-2022 | 1 | Initial release |
| 12-Dec-2023 | 2 | Added : Die information<br>Revised document presentation, minor textual updates |

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