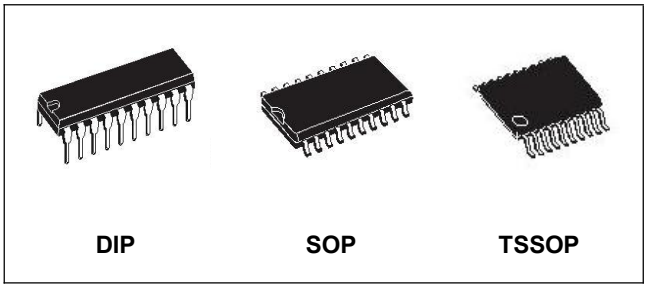
Beijing Relitech Co., LTD.

RD74HC273

OCTAL D TYPE FLIP FLOP WITH CLEAR

Datasheet- production data



DIP **SOP** **TSSOP**

Features

- HIGH SPEED:
  f_{MAX} = 66MHz (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 4μA (MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28% V_{CC}(MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 4mA (MIN.)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC}(OPR.) = 2V to 6V

Description

The RD74HC273 is a high-speed CMOS OCTAL D TYPE FLIP FLOP WITH CLEAR fabricated with silicon gate CMOS technology.

Information signals applied to D inputs are transferred to the Q outputs on the positive-going edge of the clock pulse.

When the $\overline{CLEAR}$ input is held low, the Q output are in the low logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

PART NUMBER	PACKAGE
RD74HC273BDI	DIP20
RD74HC273BSO	SOP20
RD74HC273BTS	TSSOP20

1 Pin information

Figure 1. Pin connection and IEC logic symbols

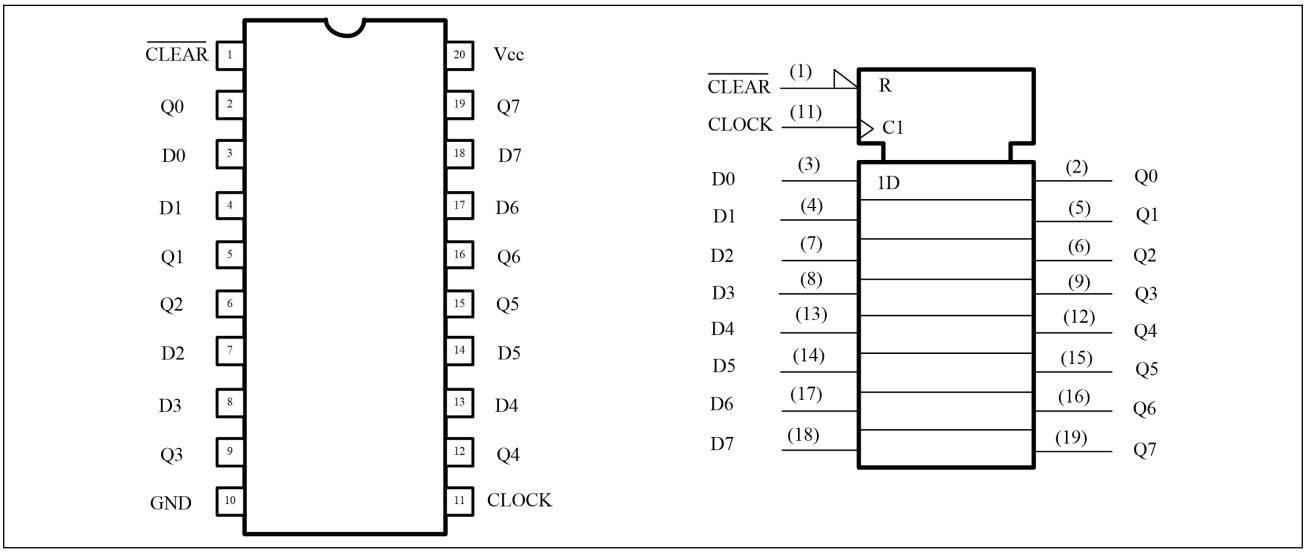


Table 2. Pin description

Pin No	Symbol	Name and function
1	$\overline{\text{CLEAR}}$	Master Reset Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	Flip Flop Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW to HIGH, Edge Triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

2 Functional description

Figure 2. Logic diagram

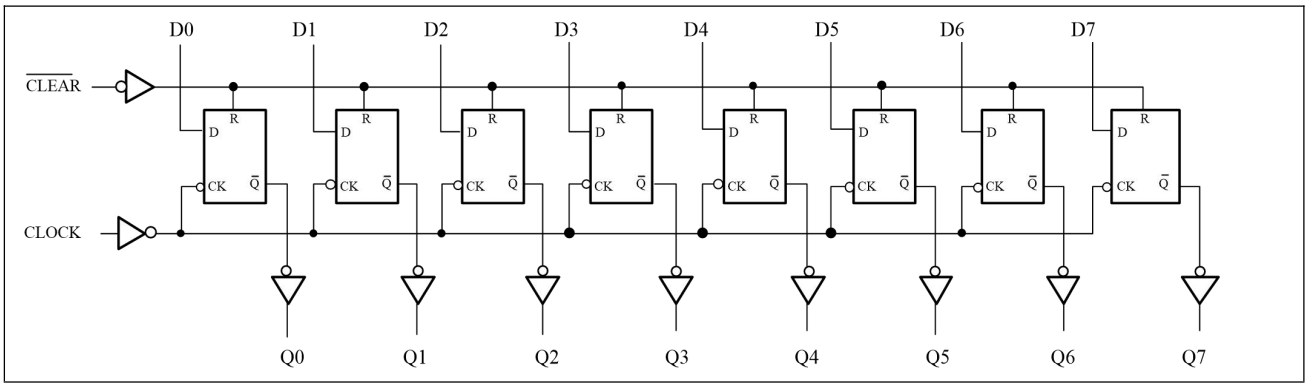
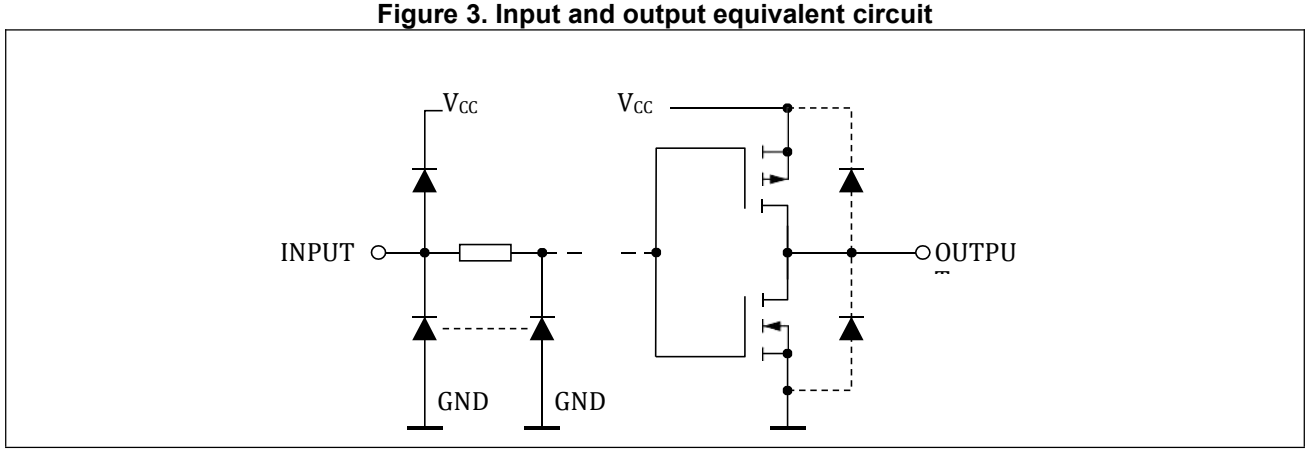


Table 3. Truth table

INPUTS			OUTPUTS	FUNCTION
$\overline{\text{CLEAR}}$	CLOCK	D	Q	
L	X	X	L	CLEAR
H	↑	L	L	
H	↑	H	H	
H	↓	X	Qn	NO CHANGE

X = Don't care

Figure 3. Input and output equivalent circuit



3 Electrical characteristics

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 7.0	V
V_I	DC Input Voltage	-0.5 to V_{CC}+ 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC}+ 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC Vcc or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to + 150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

Table 6. DC specifications

Symbol	Parameter	Test Condition		Value					Unit
		V_{cc} (V)		T_A = 25 °C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		V
		4.5		3.15			3.15		
		6.0		4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5	V
		4.5				1.35		1.35	
		6.0				1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20μA	1.9	2.0		1.9		V
		4.5	I_O=-20μA	4.4	4.5		4.4		
		6.0	I_O=-20μA	5.9	6.0		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		

Table 6. DC specifications(continued)

Symbol	Parameter	Test Condition		Value					Unit
		V_{cc} (V)		T_A = 25 °C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
V_{OL}	Low Level Output Voltage	2.0	I_O=20 μA		0.0	0.1		0.1	V
		4.5	I_O=20 μA		0.0	0.1		0.1	
		6.0	I_O=20 μA		0.0	0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33	
		6.0	I_O=5.2 mA		0.18	0.26		0.33	
I_I	Input Leakage Current	6.0	V_I = V_{CC}or GND			±0.1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I= V_{CC}or GND			4		40	μA

Table 7. AC electrical characteristics (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	Test Condition		Value					Unit
		V_{cc} (V)		T_A= 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
$t_{TLH}t_{THL}$	Output Transition Time	2.0			25	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
$t_{PLH}t_{PHL}$	Propagation Delay Time(CLOCK – Q)	2.0			54	145		180	ns
		4.5			18	29		36	
		6.0			15	25		31	
t_{PHL}	Propagation Delay Time($\overline{\text{CLEAR}}$– Q)	2.0			60	160		200	ns
		4.5			20	32		40	
		6.0			17	27		34	
f_{MAX}	Maximum Clock Frequency	2.0		6	18		4.8		MHz
		4.5		30	56		24		
		6.0		35	66		28		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width(CLOCK)	2.0			28	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
$t_{W(L)}$	Minimum Pulse Width($\overline{\text{CLEAR}}$)	2.0			28	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
t_s	Minimum Set-up Time	2.0			20	75		95	ns
		4.5			4	15		19	
		6.0			3	13		16	
t_h	Minimum Hold Time	2.0				0		0	ns
		4.5				0		0	
		6.0				0		0	
t_{REM}	Minimum Removal Time($\overline{\text{CLEAR}}$)	2.0			16	50		65	ns
		4.5			4	10		13	
		6.0			3	9		11	

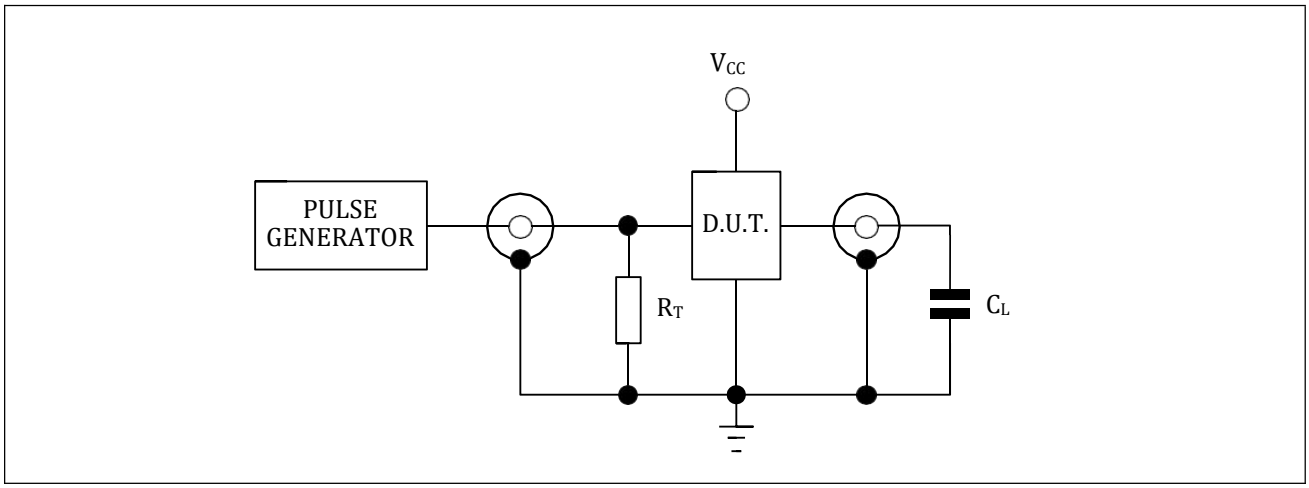
Table 8. Capacitive characteristics

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance	5.0			5	10		10	pF
C_{PD}	Power Dissipation Capacitance(1)	5.0			43				pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per FLIP FLOP), and the total CPD when n pcs of FLIP FLOP operate can be gained by the following equations: CPD (total) =32 +11 x n

4 Test circuit

Figure 4. Test circuit



C_L = 50pF or equivalent (includes jig and probe capacitance)
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 5. Waveform 1: propagation delays, setup and hold times (f=1MHz; 50% duty cycle)

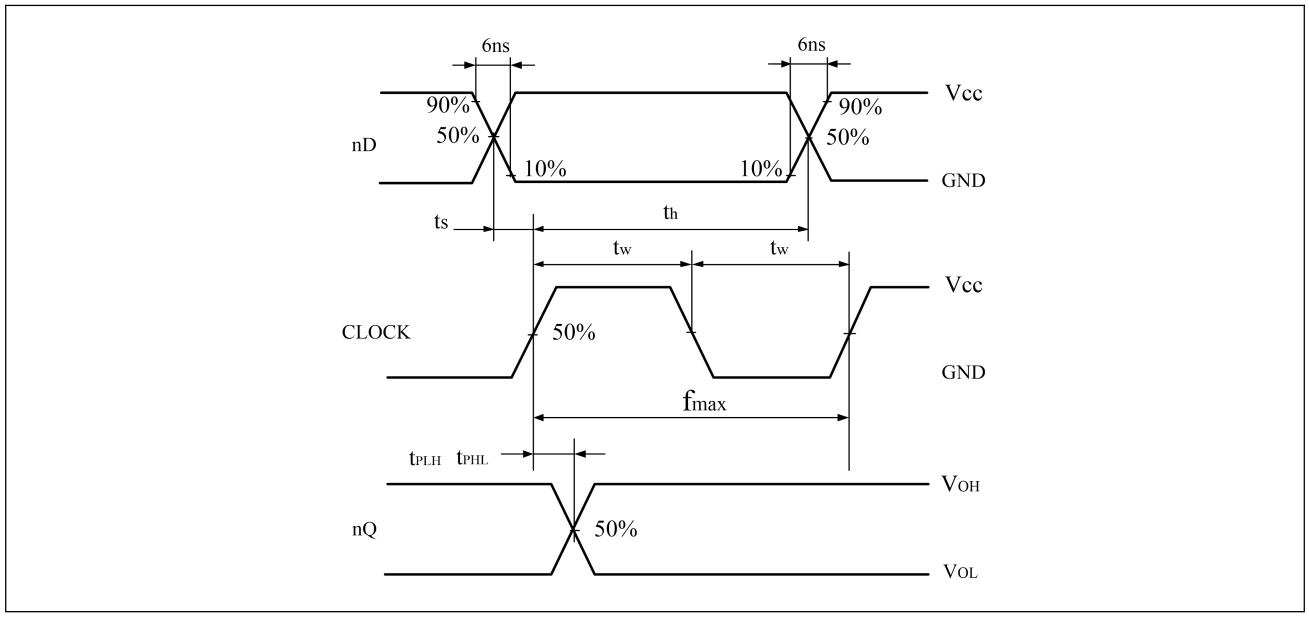
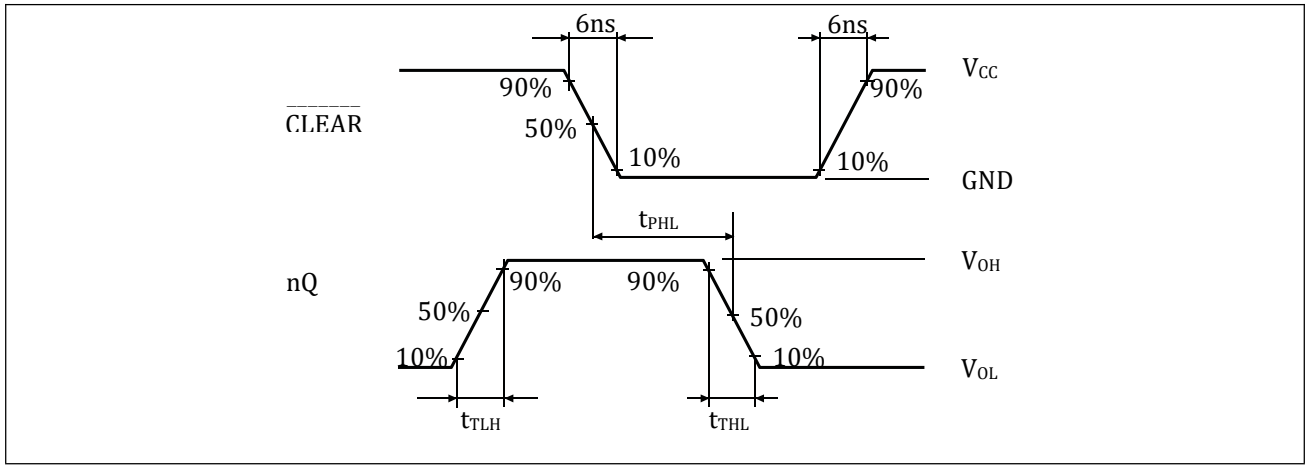
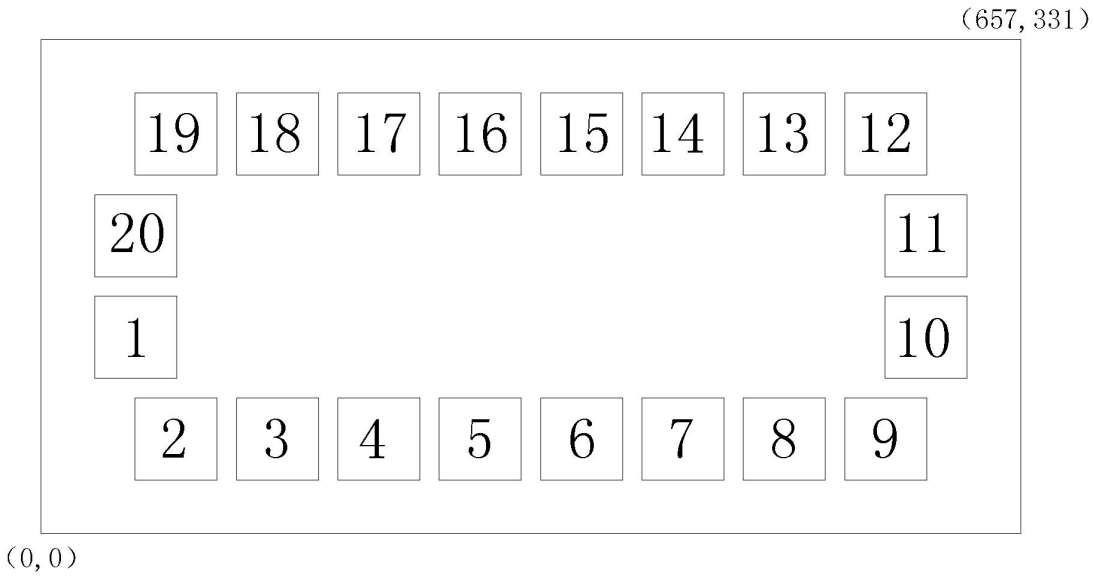


Figure 6. Waveform 2: propagation delay time (f= 1MHz; 50% duty cycle)



5 Die Information

Die Type	RD74HC273	Wafer Size	8 Inch
Die Size (μm)	X/Y: 657/331	Bond Area (μm)	X/Y: 55/55
Scribeline (μm)	60	Chip Thickness	
Metal	Front	Al+0.5%Cu	
	Back	Si	
	Top Metal Thickness	9000Å	



Pin No.	Pin Name	Coordinate		Pin No.	Pin Name	Coordinate	
		X	Y			X	Y
1	$\overline{\text{CLEAR}}$	63.5	131.5	11	CLOCK	593.5	199.5
2	Q0	90.5	63.5	12	Q4	566.5	267.5
3	D0	158.5	63.5	13	D4	498.5	267.5
4	D1	226.5	63.5	14	D5	430.5	267.5
5	Q1	294.5	63.5	15	Q5	362.5	267.5
6	Q2	362.5	63.5	16	Q6	294.5	267.5
7	D2	430.5	63.5	17	D6	226.5	267.5
8	D3	498.5	63.5	18	D7	158.5	267.5
9	Q3	566.5	63.5	19	Q7	90.5	267.5
10	GND	593.5	131.5	20	V_{CC}	63.5	199.5

6 Ordering information

Table 9. Device summary

Order code	Package	Packing
RD74HC273BDI	DIP20	Tape and reel
RD74HC273BSO	SOP20	
RD74HC273BTS	TSSOP20	
RD74HC273B		Wafer

7 Revision history

Table 10. Document revision history [1]

Date	Revision	Changes
18-Jan-2022	1	Initial release
12-Dec-2023	2	Added : Die information Revised document presentation, minor textual updates

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