Beijing Relitech Co., LTD.

RD74HC245

OCTAL BUS TRANSCEIVER
WITH 3 STATE OUTPUTS (NON INVERTED)

Datasheet- production data

DIP   SOP   TSSOP

Features

- HIGH SPEED:
  t_{PD} = 10ns (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 4µA (MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  V_{NIH} = V_{NIL} = 28% V_{CC}(MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE：
  $|I_{OH}|$ = I_{OL} = 6mA (MIN.)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC}(OPR.) = 2V to 6V

Description

The RD74HC245 is an advanced high-speed CMOS OCTAL BUS TRANSCEIVER (3-STATE) fabricated with silicon gate CMOS technology.

This IC is intended for two-way asynchronous communication between data buses, and the direction of data transmission is determined by DIR input. The enable input $\overline{G}$ can be used to disable the device so that the buses are effectively isolated.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

All floating bus terminals during High Z State must be held HIGH or LOW.

Table 1. Device summary

PART NUMBER	PACKAGE
RD74HC245BDI	DIP20
RD74HC245BSO	SOP20
RD74HC245BTS	TSSOP20

1   Pin information

Figure 1. Pin connection and IEC logic symbols
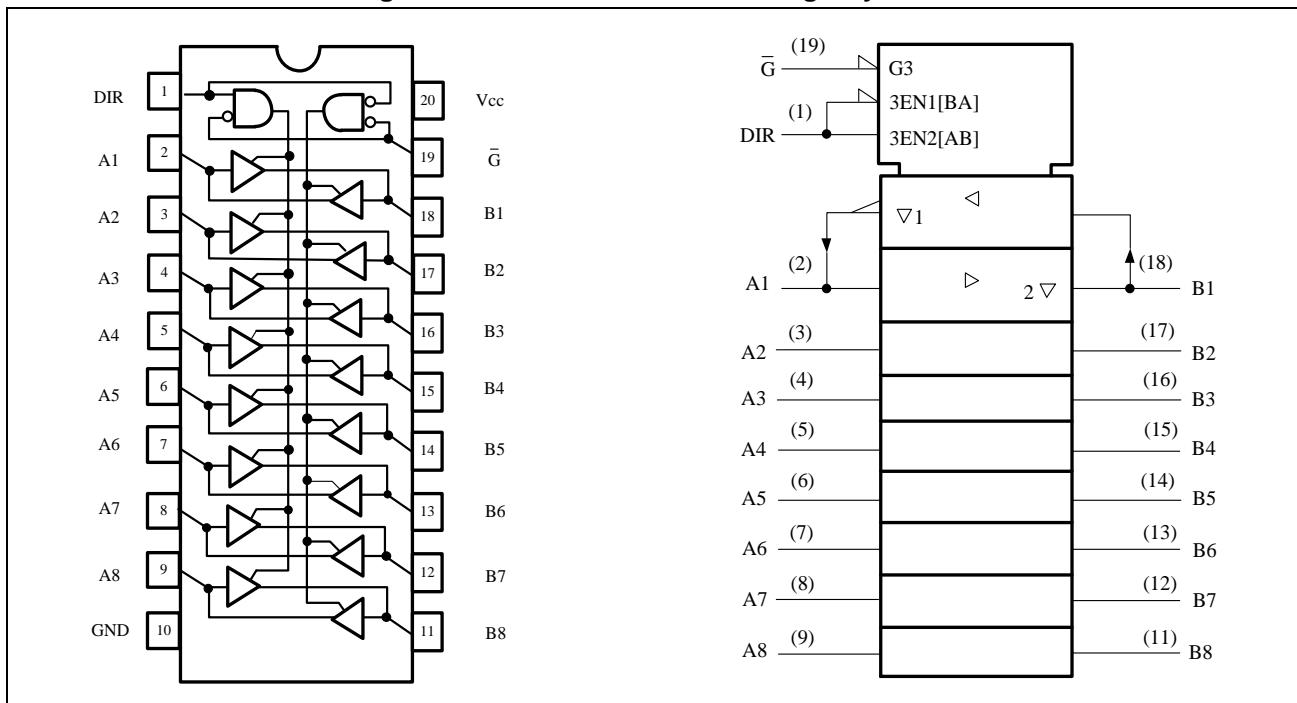
Table 2. Pin description

Pin No	Symbol	Name and function
1	DIR	Directional Control
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data Inputs/Outputs
18, 17, 16, 15, 14, 13, 12, 11	B1 to B8	Data Inputs/Outputs
19	$\overline{G}$	Output Enable Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage
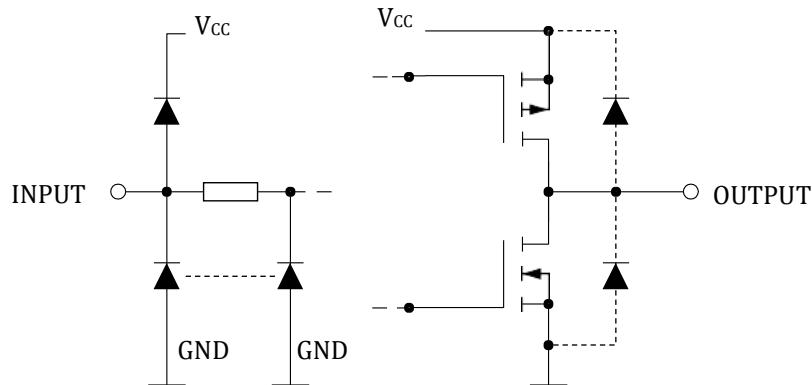
2   Functional description

Table 3. Truth table

INPUTS		FUNCTION		OUTPUT
$\overline{G}$	DIR	A BUS	B BUS	Yn
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	Z	Z	Z

X = Don't care

Z = High impedance

Figure 2. Input and output equivalent circuit

3   Electrical characteristics

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 7.0	V
V_I	DC Input Voltage	-0.5 to V_{CC}+ 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC}+ 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 35	mA
I_{CC} or I_{GND}	DC Vcc or Ground Current	± 70	mA
P_D	Power Dissipation	500 [*]	mW
T_{stg}	Storage Temperature	-65 to + 150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional
operation under these conditions is not implied
[*] 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

Table 6. DC specifications

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		$T_A = 25\ °C$			-40 to 85°C		
				Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		V
		4.5		3.15			3.15		
		6.0		4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5	V
		4.5				1.35		1.35	
		6.0				1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20μA	1.9	2.0		1.9		V
		4.5	I_O=-20μA	4.4	4.5		4.4		
		6.0	I_O=-20μA	5.9	6.0		5.9		
		4.5	I_O=-6.0 mA	4.18	4.31		4.13		
		6.0	I_O=-7.8 mA	5.68	5.8		5.63		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 μA		0.0	0.1		0.1	V
		4.5	I_O=20 μA		0.0	0.1		0.1	
		6.0	I_O=20 μA		0.0	0.1		0.1	
		4.5	I_O=6.0 mA		0.17	0.26		0.33	
		6.0	I_O=7.8 mA		0.18	0.26		0.33	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND			±0.1		±1	μA
I_{OZ}	High Impedance Output Leakage Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND			±0.5		±5	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND			4		40	μA

Table 7. AC electrical characteristics (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	Test Condition			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A= 25°C			-40 to 85°C		
					Min	Typ	Max	Min	Max	
$t_{TLH}t_{THL}$	Output Transition Time	2.0	50			25	60		75	ns
		4.5				7	12		19	
		6.0				6	10		13	
$t_{PLH}t_{PHL}$	Propagation Delay Time	2.0	50			33	90		115	ns
		4.5				12	18		23	
		6.0				10	15		20	
		2.0	150			48	120		150	ns
		4.5				16	24		30	
		6.0				14	20		26	
$t_{PZL}t_{PZH}$	High Impedance Output Enable Time	2.0	50	R_L = 1 KΩ		48	150		190	ns
		4.5		R_L = 1 KΩ		16	30		38	
		6.0				14	26		32	
		2.0	150	R_L = 1 KΩ		63	180		225	ns
		4.5		R_L = 1 KΩ		21	36		45	
		6.0				18	31		38	
$t_{PLZ}t_{PHZ}$	High Impedance Output Disable Time	2.0	50	R_L = 1 KΩ		37	150		190	ns
		4.5		R_L = 1 KΩ		17	30		38	
		6.0				15	26		32	

Table 8. Capacitive characteristics
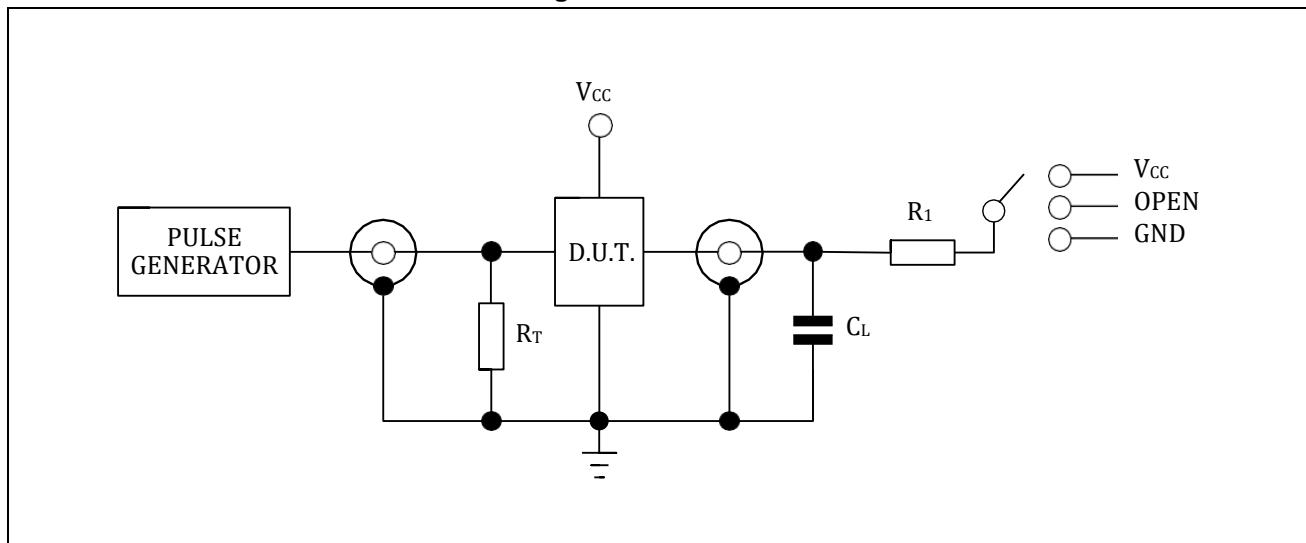
Symbol	Parameter	Test Condition			Value					Unit
		V_{CC} (V)			T_A = 25°C			-40 to 85°C		
					Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance			DIR, $\overline{G}$		5	10		10	pF
$C_{I/OUT}$	Output Capacitance			An, Bn		13				pF
C_{PD}	Power Dissipation Capacitance[1]					39				pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation:

$I_{CC(opr)}$ = C_{PD} x V_{CC} x f_{IN}+ I_{CC}/8 (per circuit)

4 Test circuit

Figure 3. Test circuit
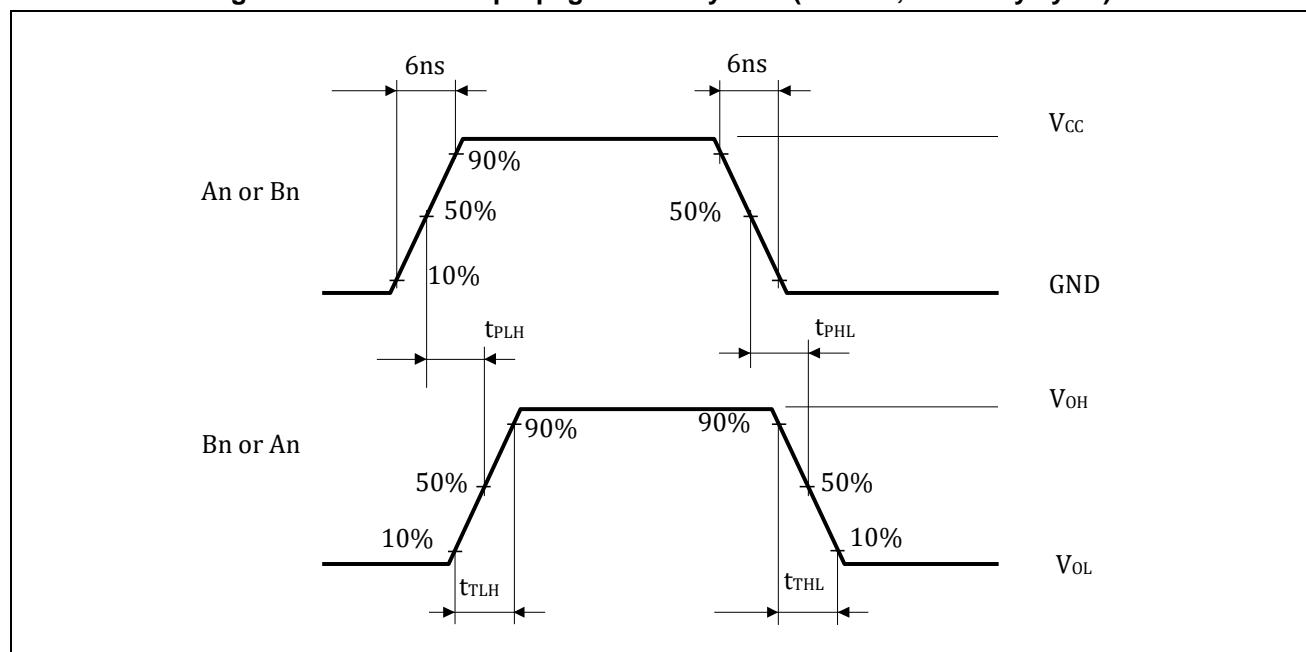
TEST	SWITCH
t_{PLH}, t_{PHL}	OPEN
t_{PZL}, t_{PLZ}	Vcc
t_{PZH}, t_{PHZ}	GND
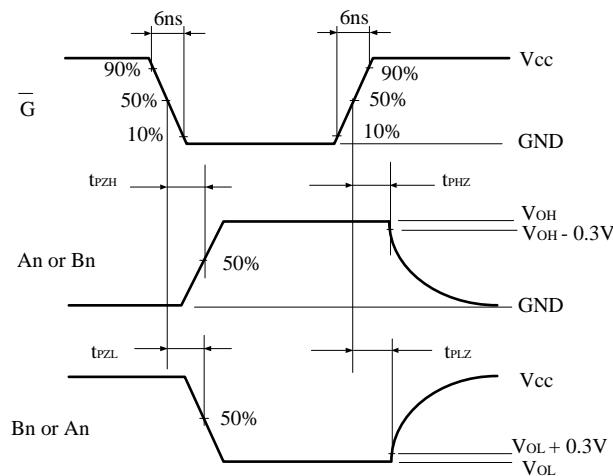
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)
R_1 = 1KΩ or equivalent
C_L = 50pF/150pF or equivalent (includes jig and probe capacitance)
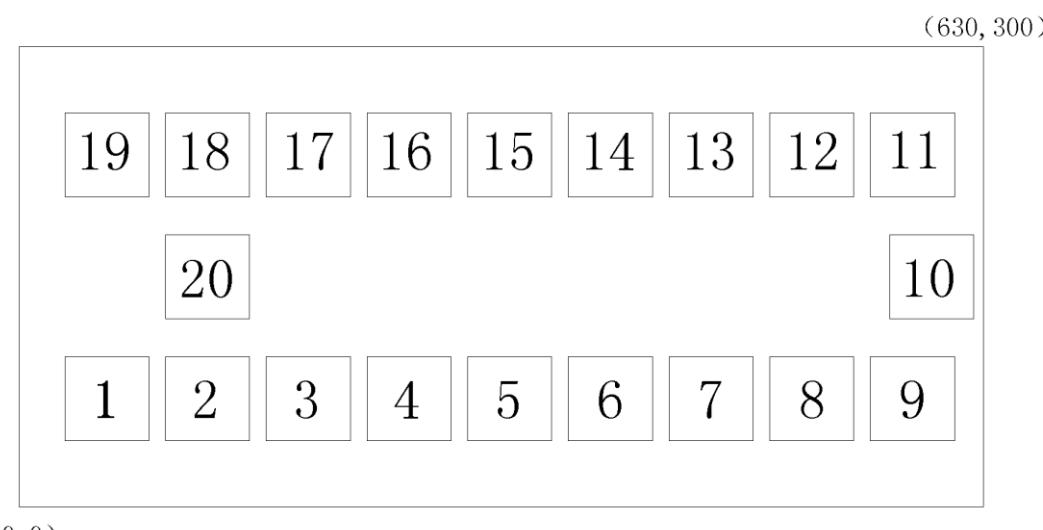
**Figure 4. Waveform 1: propagation delay time (f=1MHz; 50% duty cycle)**

Figure 5. Waveform 2: output enable and disable time (f=1MHz; 50% duty cycle)

5 Die Information

Die Type		RD74HC245	Wafer Size	8 Inch
Die Size (µm)		X/Y: 630/300	Bond Area (µm)	X/Y: 55/55
Scribeline (µm)		60	Chip Thickness	
Metal	Front		Al+0.5%Cu	
	Back		Si	
	Top Metal Thickness		12000Å	

Pin No.	Pin Name	Coordinate		Pin No.	Pin Name	Coordinate	
		X	Y			X	Y
1	DIR	57.3	70.5	11	B8	583.7	229.5
2	A1	123.1	70.5	12	B7	517.9	229.5
3	A2	188.9	70.5	13	B6	452.1	229.5
4	A3	254.7	70.5	14	B5	386.3	229.5
5	A4	320.5	70.5	15	B4	320.5	229.5
6	A5	386.3	70.5	16	B3	254.7	229.5
7	A6	452.1	70.5	17	B2	188.9	229.5
8	A7	517.9	70.5	18	B1	123.1	229.5
9	A8	583.7	70.5	19	$\overline{G}$	57.3	229.5
10	GND	596.35	150.0	20	V_{CC}	123.1	150.0

6 Ordering information

Table 9. Device summary

Order code	Package	Packing
RD74HC245BDI	DIP20	Tape and reel
RD74HC245BSO	SOP20	
RD74HC245BTS	TSSOP20	
RD74HC245B		Wafer

7 Revision history

Table 10. Document revision history [1]

Date	Revision	Changes
18-Jan-2022	1	Initial release
12-Dec-2023	2	Added : Die information Revised document presentation, minor textual updates

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