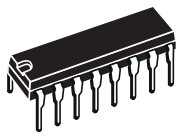
Beijing Relitech Co., LTD.

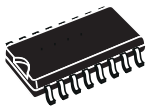
RD74HC165

8 BIT PISO SHIFT REGISTER

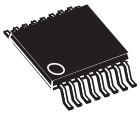
Datasheet- production data



DIP



SOP



TSSOP

Features

- HIGH SPEED:
  t_{PD} = 15ns (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 4μA (MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  V_{NIH} = V_{NIL} = 28% V_{CC}(MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}|$ = I_{OL} = 4mA (MIN.)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC}(OPR.) = 2V to 6V

Description

The RD74HC165 is a high-speed CMOS 8 BIT PISO SHIFT REGISTER fabricated with silicon gate CMOS technology.

This device contains eight clocked master slave RS flip-flops connected as a shift register, with auxiliary gating to provide over-riding asynchronous parallel entry. Parallel data enters when the shift/$\overline{load}$ input is low. The parallel data can change while shift/$\overline{load}$ is low, provided that the recommended set-up and hold times are observed. For clocked operation, shift/$\overline{load}$ must be high. The two clock input perform identically; one can be used as a clock inhibit by applying a high signal; to permit this operation clocking is accomplished through a 2 input nor gate.

To avoid double clocking, however, the inhibit signal should only go high while the clock is high. Otherwise the rising inhibit signal will cause the same response as rising clock edge.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

PART NUMBER	PACKAGE
RD74HC165BDI	DIP16
RD74HC165BSO	SOP16
RD74HC165BTS	TSSOP16

1 Pin information

Figure 1. Pin connection and IEC logic symbols

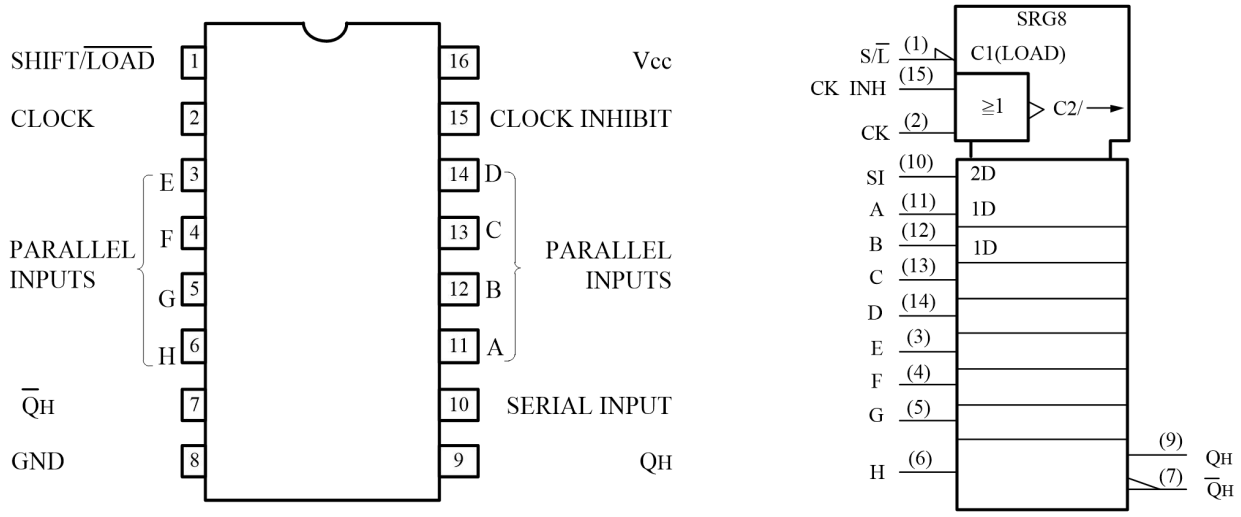
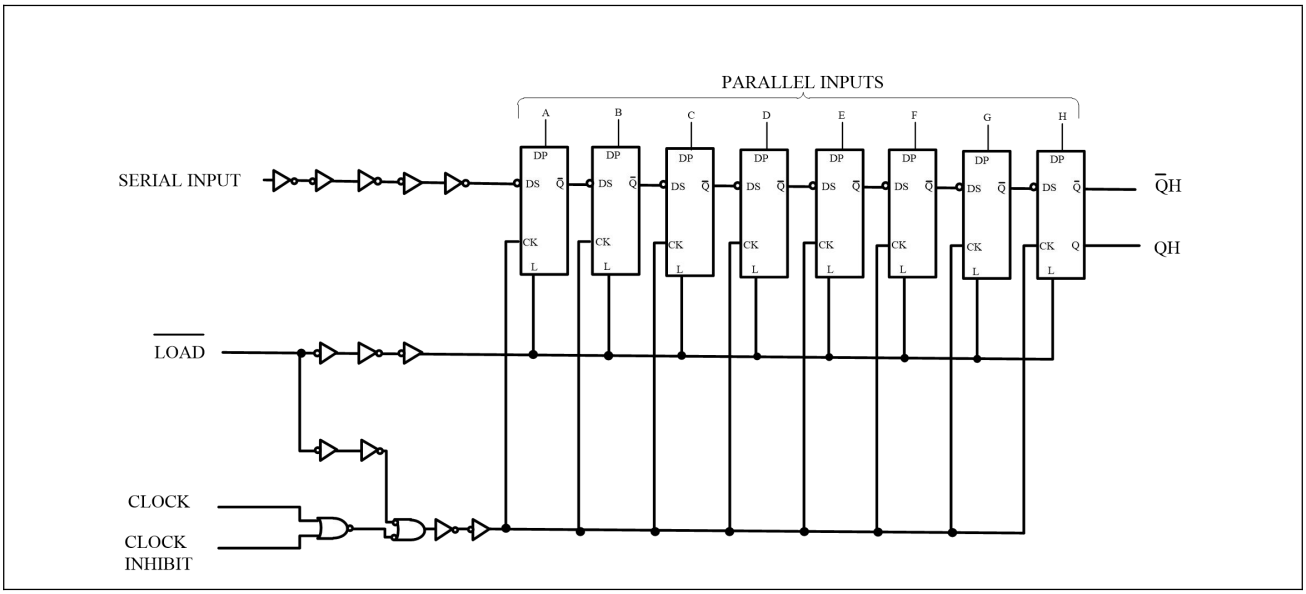


Table 2. Pin description

Pin No	Symbol	Name and function
1	SHIFT/$\overline{\text{LOAD}}$	Data Inputs
7	$\overline{\text{Q}}$H	Complementary Output
9	QH	Serial Output
2	CLOCK	Clock Input (LOW to HIGH, Edge Triggered)
10	SI	Serial Data Inputs
11, 12, 13, 14, 3, 4, 5, 6	A to H	Parallel Data Inputs
15	CLOCK INH	Clock Inhibit
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

2 Functional description

Figure2. Logic diagram



This logic diagram has not been used to estimate propagation delays

Table 3. Truth table

INPUTS					INTERNAL OUTPUTS		OUTPUTS
SHIFT/ LOAD	CLOCK INH	CLOCK	SI	A……H	QA	QB	QH
L	X	X	X	a……h	a	b	h
H	L	↑	H	X	H	QAn	QGn
H	L	↑	L	X	L	QAn	QGn
H	↑	L	H	X	H	QAn	QGn
H	↑	L	L	X	L	QAn	QGn
H	X	H	X	X	NO CHANGE		
H	H	X	X	X	NO CHANGE		

a……h: The level of steady input voltage at inputs a through respectively

QAn - QGn : The level of QA - QG, respectively. before the most-recent transition of the clock

Figure 3. Input and output equivalent circuit

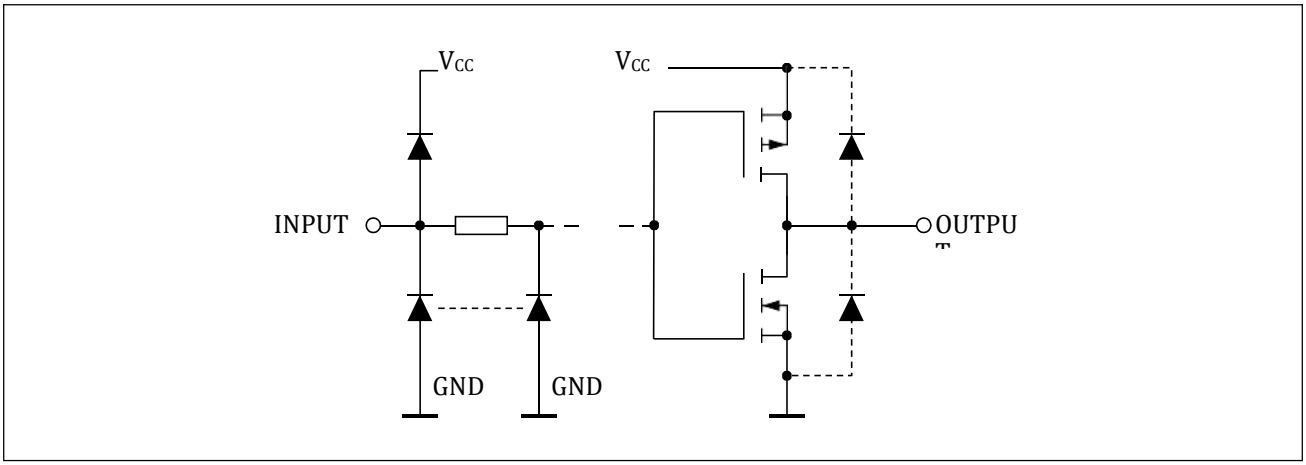
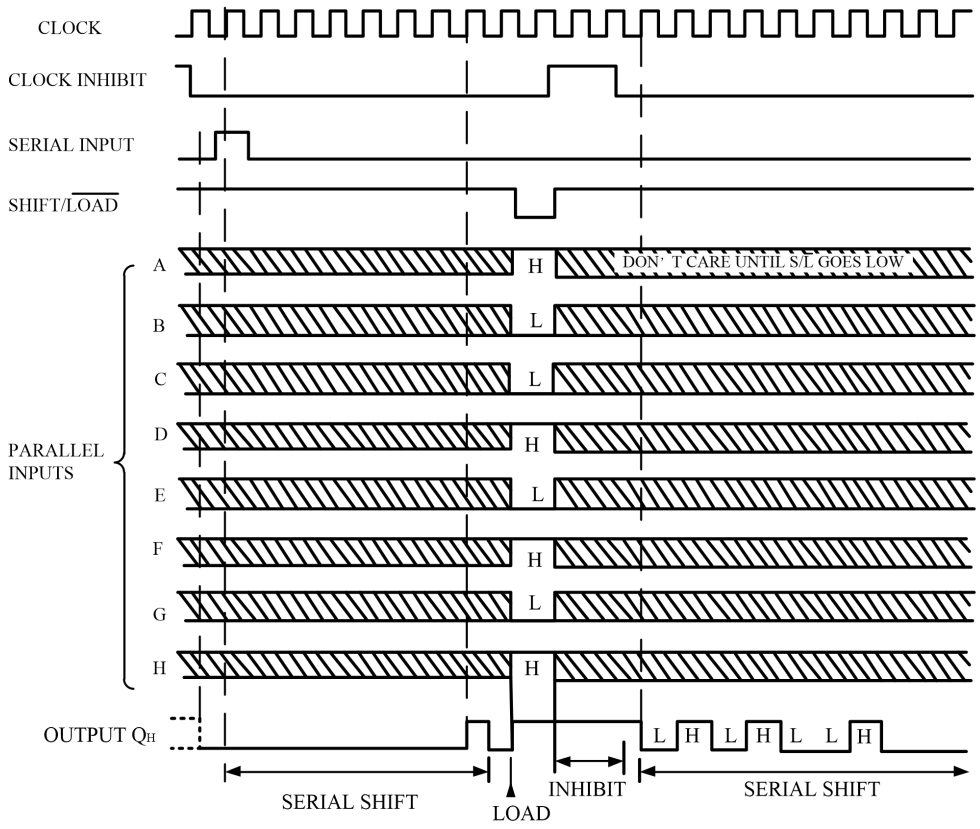


Figure 4. Timing chart



3 Electrical characteristics

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 7.0	V
V_I	DC Input Voltage	-0.5 to V_{CC}+ 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC}+ 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC}or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to + 150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

Table 6. DC specifications

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		V
		4.5		3.15			3.15		
		6.0		4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5	V
		4.5				1.35		1.35	
		6.0				1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20μA	1.9	2.0		1.9		V
		4.5	I_O=-20μA	4.4	4.5		4.4		
		6.0	I_O=-20μA	5.9	6.0		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 μA		0.0	0.1		0.1	V
		4.5	I_O=20 μA		0.0	0.1		0.1	
		6.0	I_O=20 μA		0.0	0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33	
		6.0	I_O=5.2 mA		0.18	0.26		0.33	
I_I	Input Leakage Current	6.0	V_I = V_{CC}or GND			± 0.1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I= V_{CC}or GND			4		40	μA

Table 7. AC electrical characteristics (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A= 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
t_{PLH} t_{PHL}	Propagation Delay Time(CLOCK – QH, $\overline{QH}$)	2.0			55	150		190	ns
		4.5			18	30		38	
		6.0			15	26		33	
t_{PLH} t_{PHL}	Propagation Delay Time(SHIFT/$\overline{LOAD}$– QH, $\overline{QH}$)	2.0			65	165		205	ns
		4.5			21	33		41	
		6.0			18	28		35	
t_{PLH} t_{PHL}	Propagation Delay Time(H – QH, $\overline{QH}$)	2.0			52	135		170	ns
		4.5			17	27		34	
		6.0			14	23		29	
f_{MAX}	Maximum Clock Frequency	2.0		7.4	15		6.0		MHz
		4.5		37	60		30		
		6.0		44	71		35		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width(CLOCK)	2.0			24	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
$t_{W(L)}$	Minimum Pulse Width(SHIFT/$\overline{LOAD}$)	2.0			32	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
t_s	Minimum Set-up Time (PI - SHIFT/$\overline{LOAD}$) (SI – CLOCK) (SHIFT/$\overline{LOAD}$ - CK)	2.0			24	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
t_h	Minimum Hold Time (PI - SHIFT/$\overline{LOAD}$) (SI – CLOCK) (SHIFT/$\overline{LOAD}$ - CK)	2.0				0		0	ns
		4.5				0		0	
		6.0				0		0	
t_{REM}	Minimum Removal Time (CLOCK – CK INH)	2.0			20	75		95	ns
		4.5			5	15		19	
		6.0			4	13		16	

Table 8. Capacitive characteristics

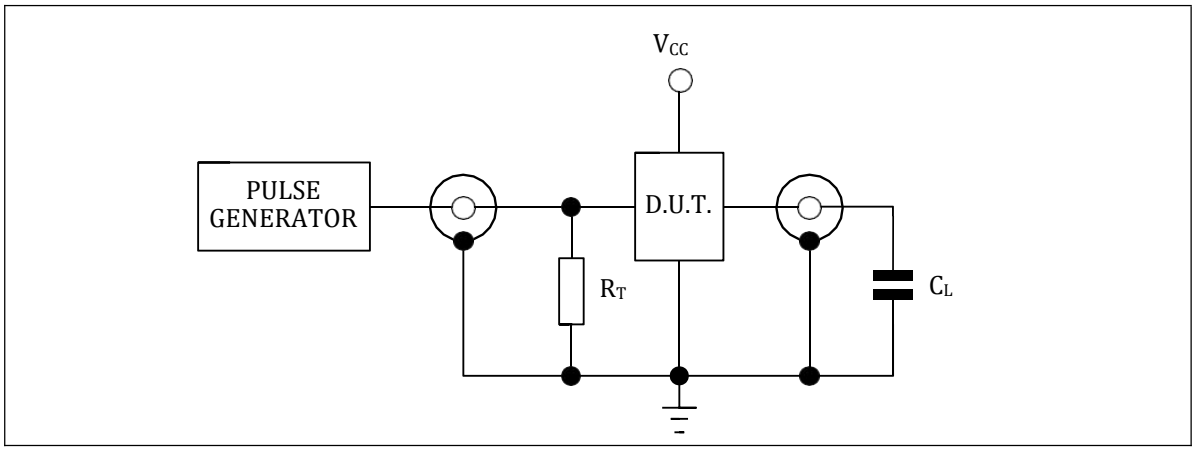
Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance	5.0			5	10		10	pF
C_{PD}	Power Dissipation Capacitance(1)	5.0			55				pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation:

   $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

4 Test circuit

Figure 5. Test circuit



R_T = Z_{OUT} of pulse generator (typically 50Ω)
C_L = 50pF or equivalent (includes jig and probe capacitance)

Figure 6. Waveform 1: serial mode propagation delay (f=1MHz; 50% duty cycle)

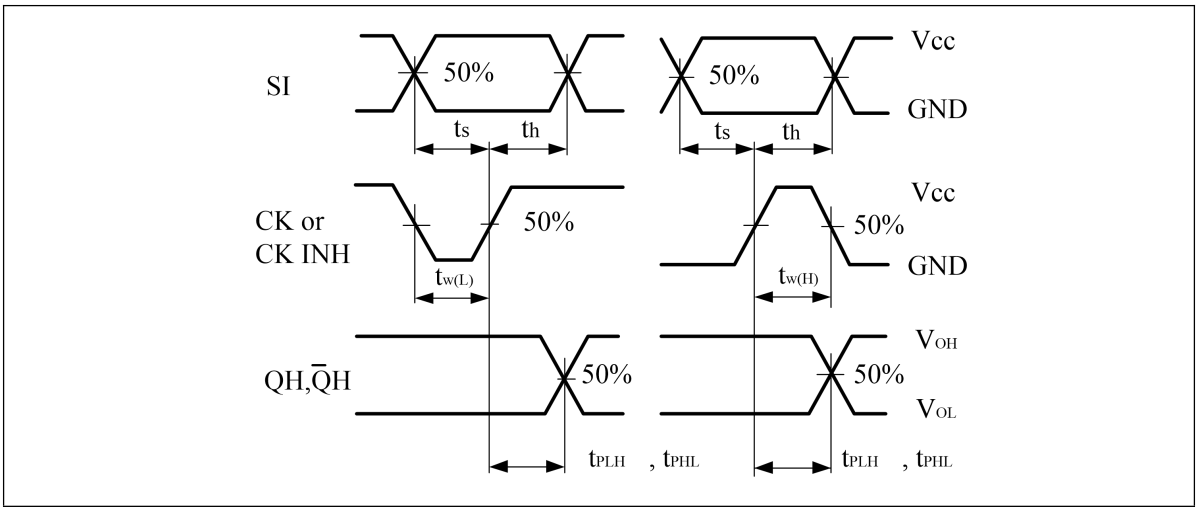


Figure 7. Waveform 2:parallel mode propagation delay (f=1MHz; 50% duty cycle)

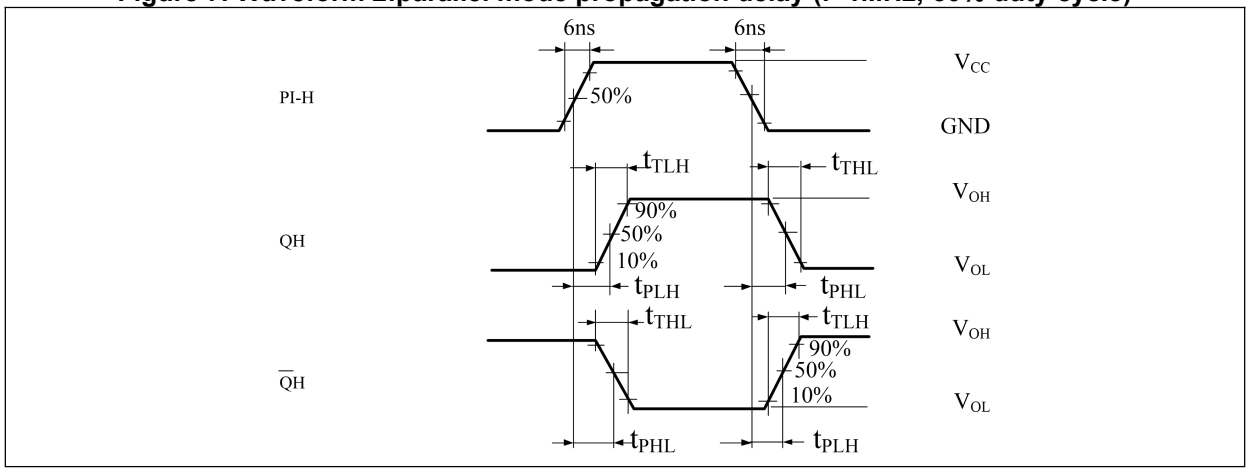


Figure 8. Waveform 3:minimum pulse width(S/$\overline{L}$), propagation delay times (f= 1MHz; 50% duty cycle)

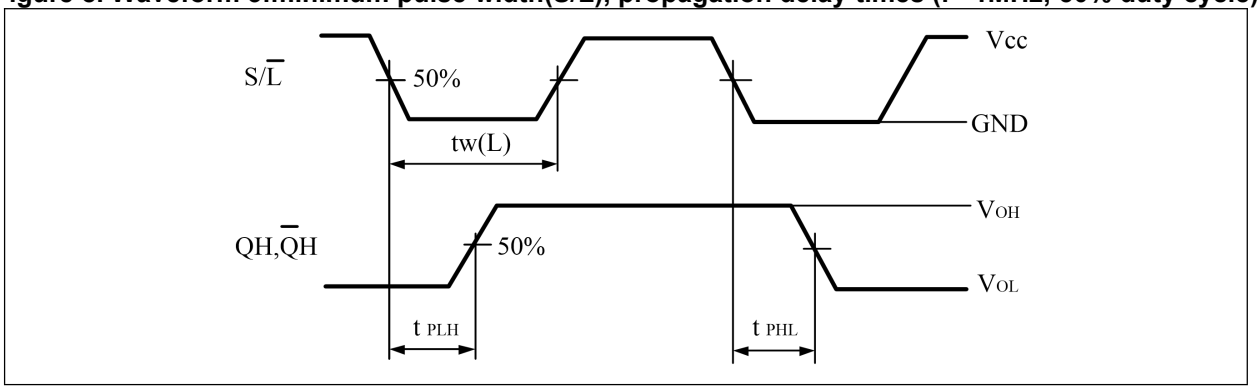


Figure 9. Waveform 4:setup and hold time (PI to S/$\overline{L}$) (f= 1MHz; 50% duty cycle)

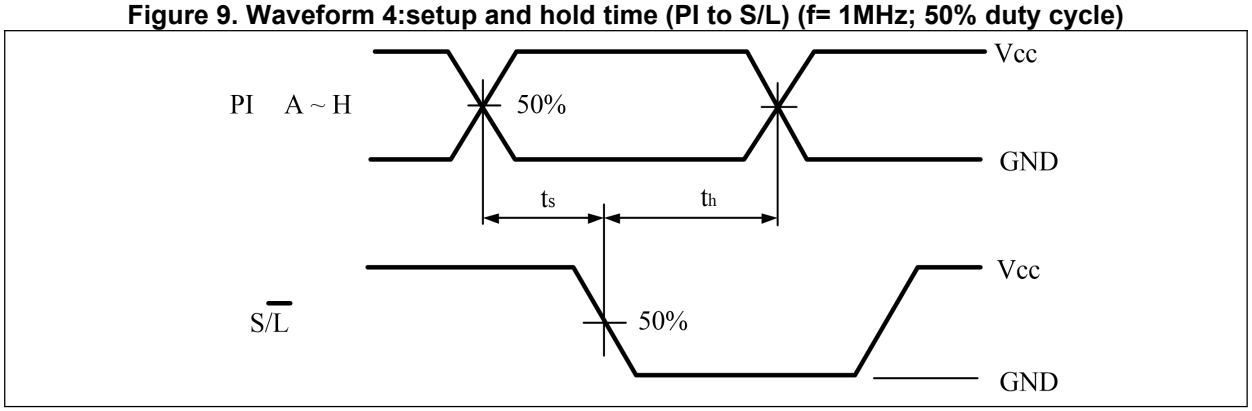
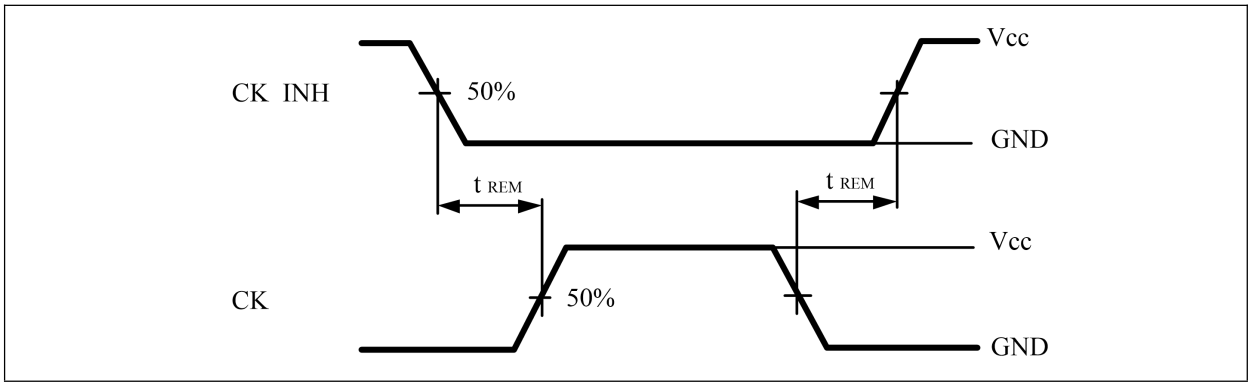
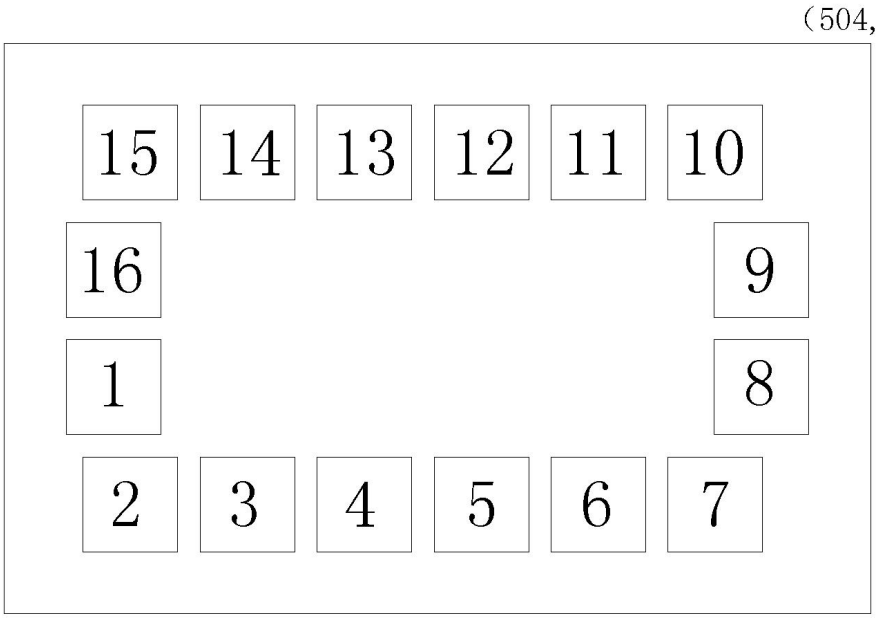


Figure 10. Waveform 5: minimum removal time (CK INH to CK) (f= 1MHz; 50% duty cycle)



5 Die Information

Die Type	RD74HC165	Wafer Size	8 Inch
Die Size (μm)	X/Y: 504/331	Bond Area (μm)	X/Y: 55/55
Scribeline (μm)	60	Chip Thickness	
Metal	Front	Al+0.5%Cu	
	Back	Si	
	Top Metal Thickness	9000Å	



Pin No.	Pin Name	Coordinate		Pin No.	Pin Name	Coordinate	
		X	Y			X	Y
1	SHIFT/$\overline{\text{LOAD}}$	63.5	131.5	9	QH	440.5	199.5
2	CLOCK	73.5	63.5	10	SL	413.5	267.5
3	E	141.5	63.5	11	A	345.5	267.5
4	F	209.5	63.5	12	B	277.5	267.5
5	G	277.5	63.5	13	C	209.5	267.5
6	H	345.5	63.5	14	D	141.5	267.5
7	$\overline{\text{QH}}$	413.5	63.5	15	CLOCK INH	73.5	267.5
8	GND	440.5	131.5	16	V_{CC}	63.5	199.5

6 Ordering information

Table 9. Device summary

Order code	Package	Packing
RD74HC165BDI	DIP16	Tape and reel
RD74HC165BSO	SOP16	
RD74HC165BTS	TSSOP16	
RD74HC165B		Wafer

7 Revision history

Table 10. Document revision history (1)

Date	Revision	Changes
18-Jan-2022	1	Initial release
12-Dec-2023	2	Added : Die information Revised document presentation, minor textual updates

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