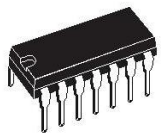
Beijing Relitech Co., LTD.

RD74HC164

8 BIT SIPO SHIFT REGISTER

Datasheet- production data



DIP **SOP** **TSSOP**

Features

- HIGH SPEED:
  f_{MAX} = 62MHz (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 4µA (MAX.) at T_A= 25°C
- HIGH NOISE IMMUNITY:
  V_{NIH} = V_{NIL} = 28% V_{CC}(MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}|$ = I_{OL} = 4mA (MIN.)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC}(OPR.) = 2V to 6V

Description

The RD74HC164 is a high-speed CMOS 8 BIT SIPO SHIFT REGISTER fabricated with silicon gate CMOS technology.

The RD74HC164 is an 8 bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B), either of these inputs can be used as an active high enable for data entry through the other input. An unused input must be high, or both inputs connected together. Each low-to-high transition on the clock inputs shifts data one place to the right and enters into QA the logic NAND of the two data inputs ($\overline{A \times B}$), the data that existed before the rising clock edge. A low level on the clear input overrides all other inputs and clears the register asynchronously, forcing all Q outputs low. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

PART NUMBER	PACKAGE
RD74HC164BDI	DIP14
RD74HC164BSO	SOP14
RD74HC164BTS	TSSOP14

1 Pin information

Figure 1. Pin connection and IEC logic symbols

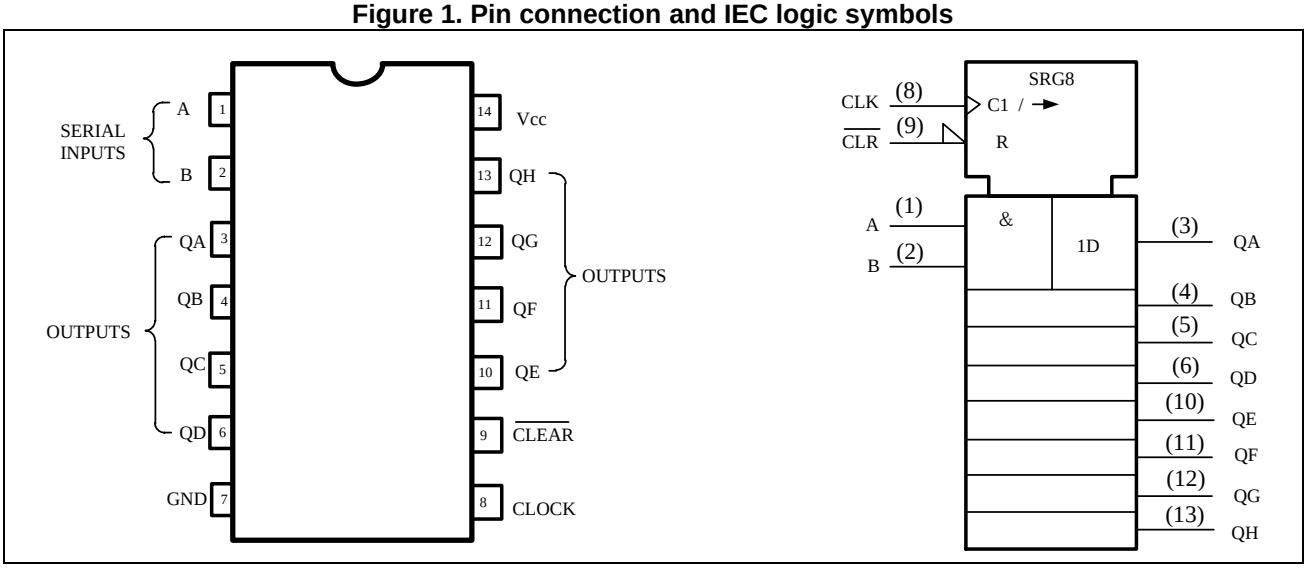
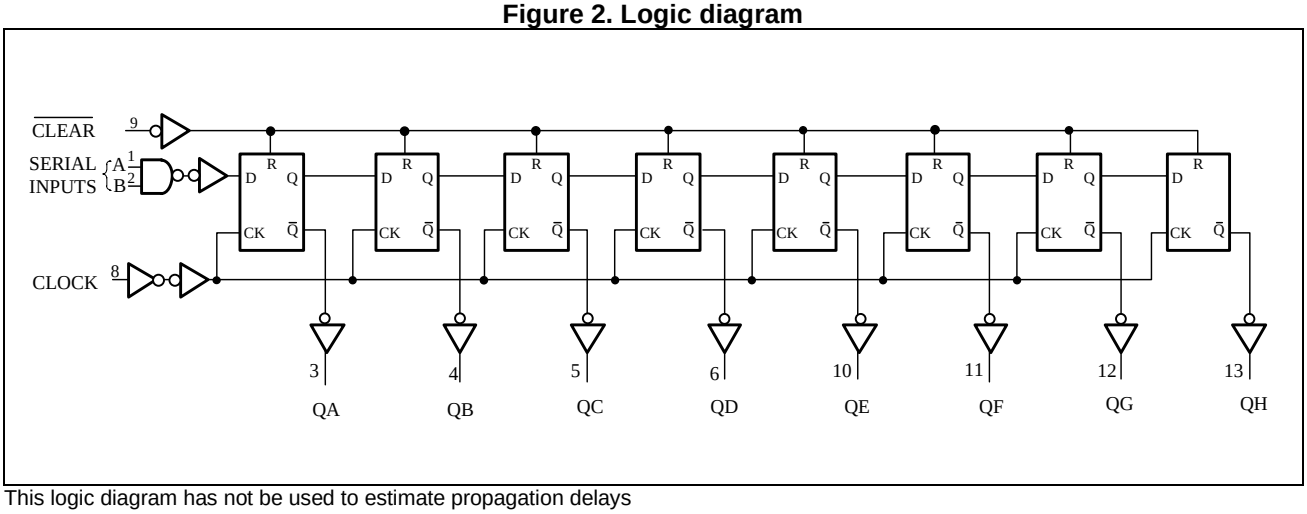


Table 2. Pin description

Pin No	Symbol	Name and function
1, 2	A, B	Data Inputs
3, 4, 5, 6, 10, 11, 12, 13	QA to QH	Outputs
8	CLOCK	Clock Input (LOW to HIGH, Edge Triggered)
9	$\overline{\text{CLEAR}}$	Master Reset Input
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

2 Functional description

Figure 2. Logic diagram



This logic diagram has not be used to estimate propagation delays

Table 3. Truth table

INPUTS				OUTPUTS			
$\overline{\text{CLEAR}}$	CLOCK	SERIAL IN		QA	QB	……	QH
		A	B				
L	X	X	X	L	L	……	L
H	↓	X	X	NO CHANGE			
H	↑	L	X	L	QAn	……	QGn
H	↑	X	L	L	QAn	……	QGn
H	↑	H	H	H	QAn	……	QGn

X:Don't Care.

QAn – QGn: The level of QA – QG, respectively, before the most-recent transition of the clock.

Figure 3. Input and output equivalent circuit

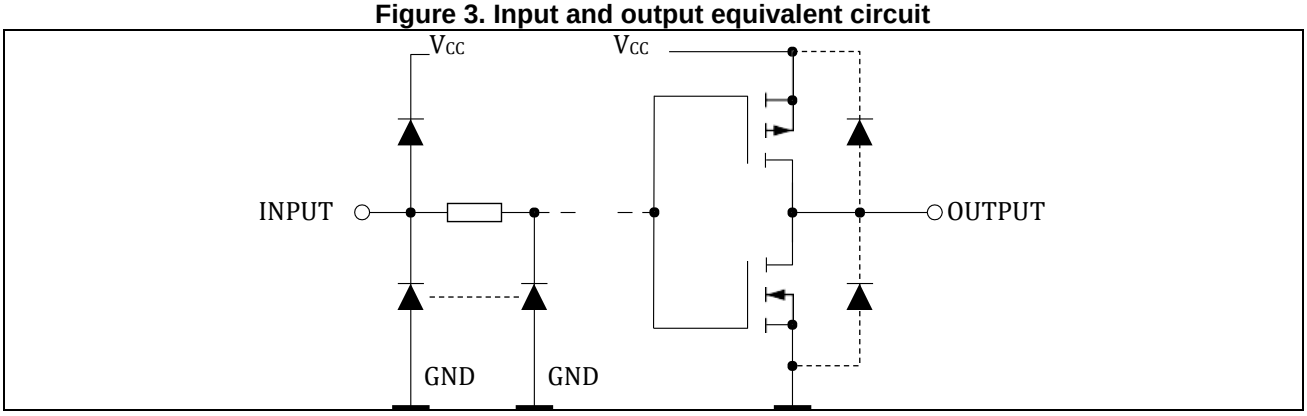
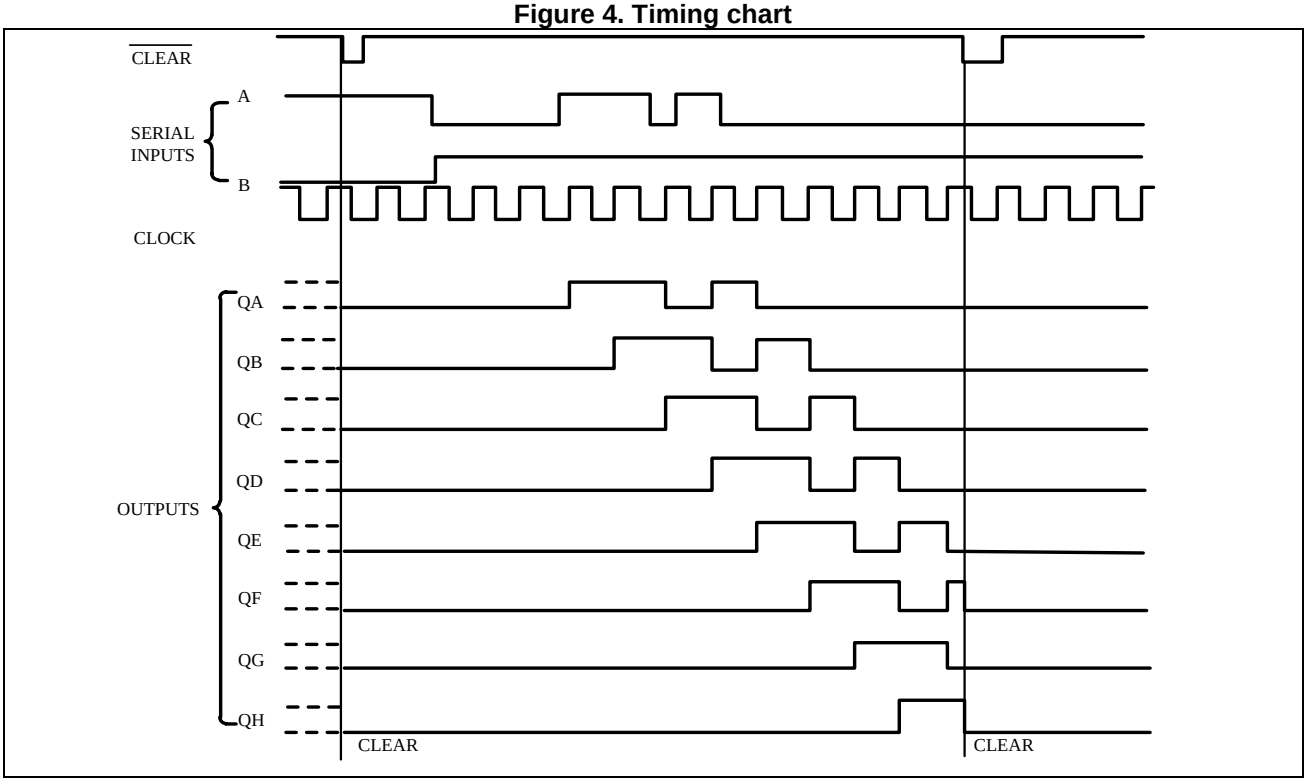


Figure 4. Timing chart



3 Electrical characteristics

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 7.0	V
V_I	DC Input Voltage	-0.5 to V_{CC}+ 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC}+ 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC}or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to + 150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

Table 6. DC specifications

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		V
		4.5		3.15			3.15		
		6.0		4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5	V
		4.5				1.35		1.35	
		6.0				1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20μA	1.9	2.0		1.9		V
		4.5	I_O=-20μA	4.4	4.5		4.4		
		6.0	I_O=-20μA	5.9	6.0		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 μA		0.0	0.1		0.1	V
		4.5	I_O=20 μA		0.0	0.1		0.1	
		6.0	I_O=20 μA		0.0	0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33	
		6.0	I_O=5.2 mA		0.18	0.26		0.33	
I_I	Input Leakage Current	6.0	V_I = V_{CC}or GND			±0.1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I= V_{CC}or GND			4		40	μA

Table 7. AC electrical characteristics (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A= 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
$t_{TLH}t_{THL}$	Output Transition Time	2.0			30	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
$t_{PLH}t_{PHL}$	Propagation Delay Time(CLOCK – Q)	2.0			57	160		200	ns
		4.5			19	32		40	
		6.0			16	27		34	
$t_{PLH}t_{PHL}$	Propagation Delay Time($\overline{CLEAR}$ – Q)	2.0			60	175		220	ns
		4.5			20	35		44	
		6.0			17	30		37	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	18		5.0		MHz
		4.5		31	53		25		
		6.0		37	62		30		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width(CLOCK)	2.0			24	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
$t_{W(L)}$	Minimum Pulse Width($\overline{CLEAR}$)	2.0			40	75		95	ns
		4.5			10	15		19	
		6.0			9	13		16	
t_s	Set-up Time(A, B -CK)	2.0		50			65		ns
		4.5		10			13		
		6.0		9			11		
t_h	Hold Time(A, B - CK)	2.0		5			5		ns
		4.5		5			5		
		6.0		5			5		
t_{REM}	Minimum Removal Time	2.0				5		5	ns
		4.5				5		5	
		6.0				5		5	

Table 8. Capacitive characteristics

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance	5.0			5	10		10	pF
C_{PD}	Power Dissipation Capacitance(1)	5.0			99				pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

4 Test circuit

Figure 5. Test circuit

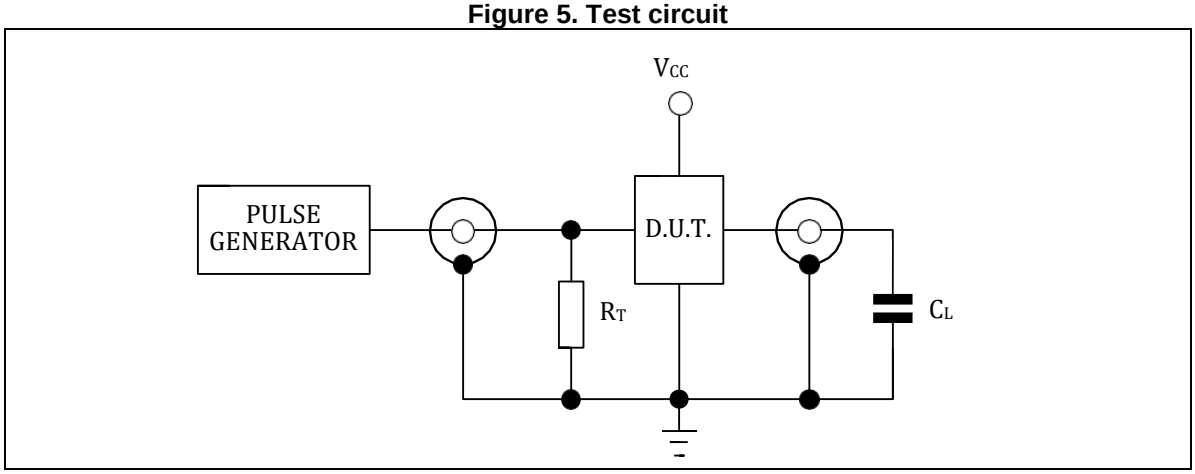


Figure 6. Waveform 1: minimum pulse width ($\overline{\text{CLEAR}}$), minimum removal time ($\overline{\text{CLEAR}}$ to CLOCK) (f= 1MHz; 50% duty cycle)

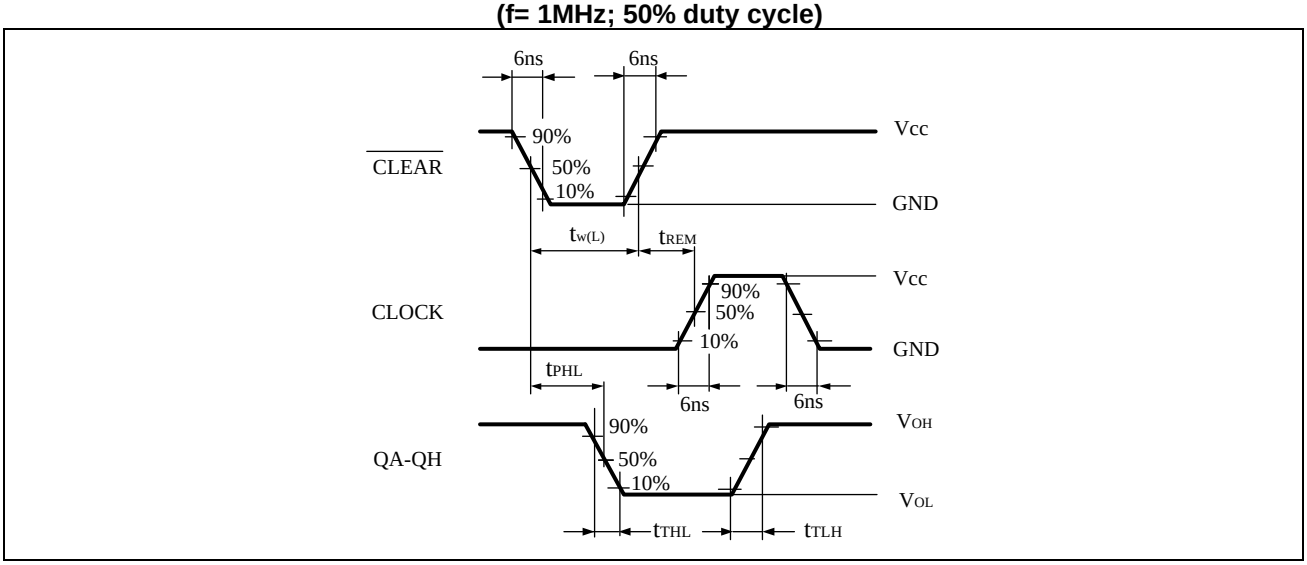
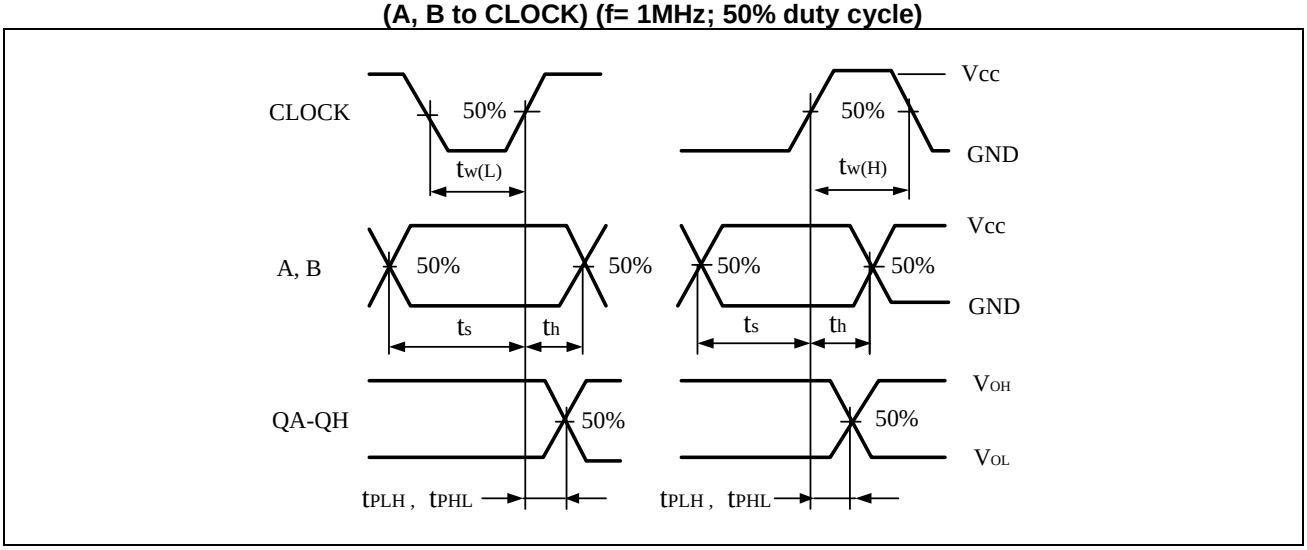
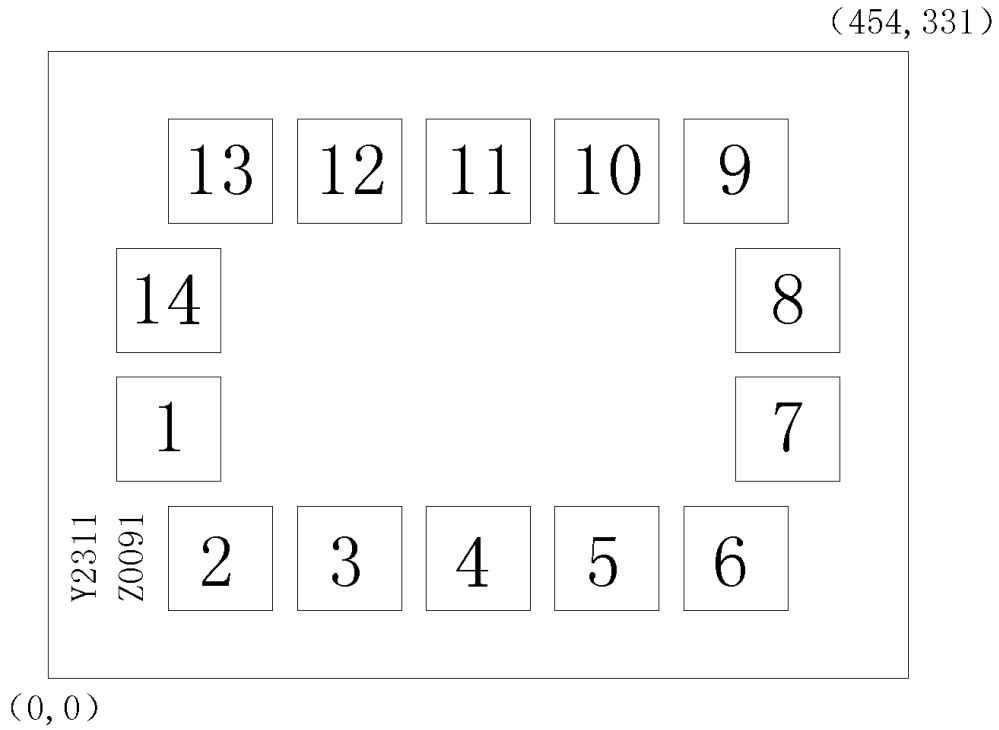


Figure 7. Waveform 2: propagation delay times, minimum pulse width (CLOCK), setup and hold time (A, B to CLOCK) (f= 1MHz; 50% duty cycle)



5 Die Information

Die Type	RD74HC164	Wafer Size	8 Inch
Die Size (μm)	X/Y:454/331	Bond Area (μm)	X/Y: 55/55
Scribeline (μm)	60	Chip Thickness	
Metal	Front	Al+0.5%Cu	
	Back	Si	
	Top Metal Thickness	9000Å	



Pin No.	Pin Name	Coordinate			Pin No.	Pin Name	Coordinate	
		X	Y				X	Y
1	A	63.5	131.5		8	CLOCK	390.5	199.5
2	B	91.0	63.5		9	$\overline{\text{CLEAR}}$	363.0	267.5
3	QA	159.0	63.5		10	QE	295.0	267.5
4	QB	227.0	63.5		11	QF	227.0	267.5
5	QC	295.0	63.5		12	QG	159.0	267.5
6	QD	363.0	63.5		13	QH	91.0	267.5
7	GND	390.5	131.5		14	V_{CC}	63.5	199.5

6 Ordering information

Table 9. Device summary

Order code	Package	Packing
RD74HC164BDI	DIP14	Tape and reel
RD74HC164BSO	SOP14	
RD74HC164BTS	TSSOP14	
RD74HC164B		Wafer

7 Revision history

Table 10. Document revision history (1)

Date	Revision	Changes
18-Jan-2022	1	Initial release
12-Dec-2023	2	Added : Die information Revised document presentation, minor textual updates

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