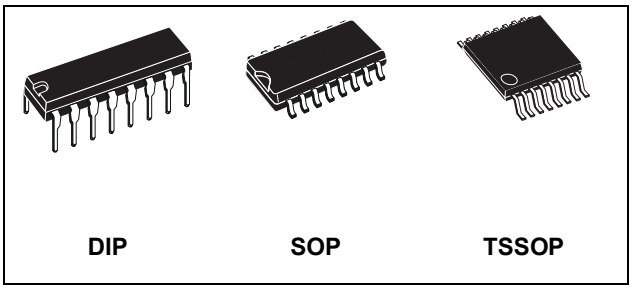
Beijing Relitech Co., LTD.

RD74HC138

3 TO 8 LINE DECODER (INVERTING)

Datasheet- production data



DIP **SOP** **TSSOP**

Features

- HIGH SPEED:
  t_{PD} = 16ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION:
  I_{CC} = 4μA at T_A=25°C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS:
  t_{PLH}=t_{PHL}
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}|$ = I_{OL}
- HIGH NOISE IMMUNITY:
  V_{NIH} = V_{NIL} = 28% V_{CC}(MIN.)
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC}(OPR.) = 2V to 6V

Description

The RD74HC138 is a high speed CMOS 3 TO 8 LINE DECODER fabricated in silicon gate CMOS technology.

It has the same high-speed performance of LSTTL combined with true CMOS low power consumption. If the device is enabled, 3 binary select inputs (A, Band C) determine which one of the outputs will go low. If enable input G1 is held low or either $\overline{G2A}$ or $\overline{G2B}$ is held high, the decoding function is inhibited and all the 8 outputs go high.

Three enable inputs are provided to ease cascade connection and application of address decoders for memory systems.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

PART NUMBER	PACKAGE
RD74HC138BDI	DIP16
RD74HC138BSO	SOP16
RD74HC138BTS	TSSOP16

1 Pin information

Figure 1. Pin connection and IEC logic symbols

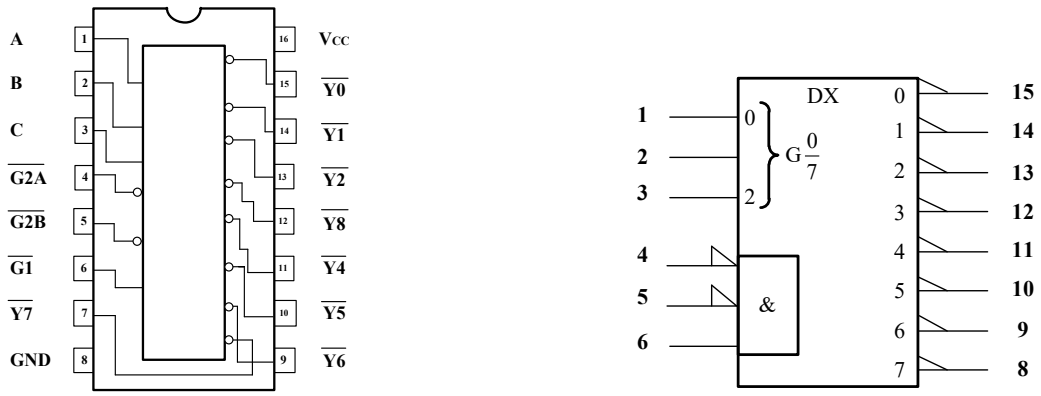


Table 2. Pin description

Pin No	Symbol	Name and function
1, 2, 3	A, B, C	Address Inputs
4, 5	$\overline{G2A}$ to $\overline{G2B}$	Enable Inputs
6	G1	Enable Input
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y0}$ to $\overline{Y7}$	Outputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

2 Functional description

Figure 2. Logic diagram

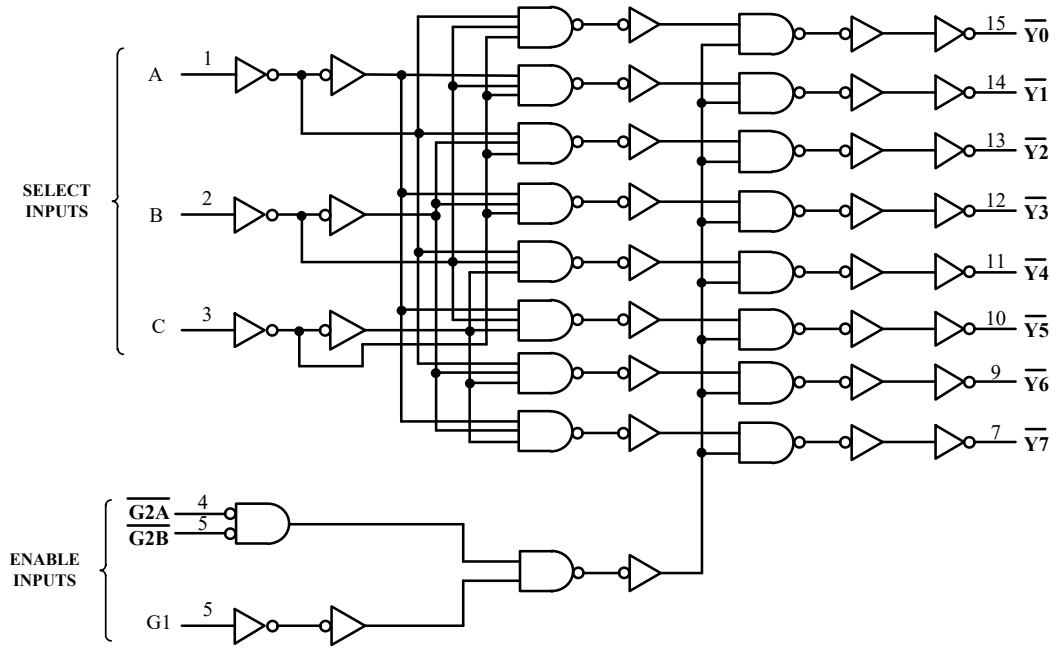
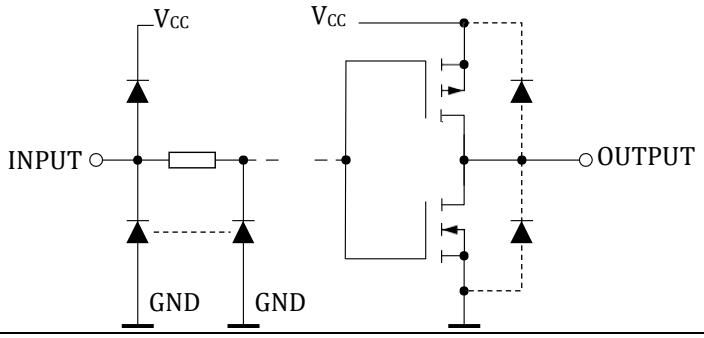


Table 3. Truth table

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G2B}$	$\overline{G2A}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

X: Don't Care

Figure 3. Input and output equivalent circuit



3 Absolute maximum ratings and operating conditions

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 7.0	V
V_I	DC Input Voltage	-0.5 to V_{CC}+ 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC}or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature:		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test Condition			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85°C		
					Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		V
		4.5			3.15			3.15		
		6.0			4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5	V
		4.5					1.35		1.35	
		6.0					1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I=V_{IH} or V_{IL}	I_O=-20μA	1.9	2.0	1.9			V
		4.5			4.4	4.5	4.4			
		6.0			5.9	6.0	5.9			
		4.5		I_O=-4.0 mA	4.18	4.31	4.13			
		6.0		I_O=-5.2 mA	5.68	5.8	5.63			
V_{OL}	Low Level Output Voltage	2.0	V_I=V_{IH} or V_{IL}	I_O=20 μA		0.0		0.1	0.1	V
		4.5				0.0		0.1	0.1	
		6.0				0.0		0.1	0.1	
		4.5		I_O=4.0 mA		0.17		0.33	0.40	
		6.0		I_O=5.2 mA		0.18		0.33	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC}or GND				±0.1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I= V_{CC}or GND				4		40	mA

Table 7. AC electrical characteristics (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A= 25°C			-40 to 85°C		
				Min.	Typ.	Max	Min.	Max	
$t_{TLH}t_{THL}$	Output Transition Time	2.0			30	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
$t_{PLH}t_{PHL}$	Propagation Delay Time (A, B - Y)	2.0			60	125		155	ns
		4.5			15	25		31	
		6.0			13	21		26	
$t_{PLH}t_{PHL}$	Propagation Delay Time ($\overline{G}$ - Y)	2.0			56	120		150	ns
		4.5			14	24		30	
		6.0			12	20		26	

Table 8. Capacitive characteristics

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance				5	10		10	pF
C_{PD}	Power Dissipation Capacitance(1)				47				pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation:
   $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

5 Test circuit

Figure 4. Test circuit I_{CC} (Opr.)

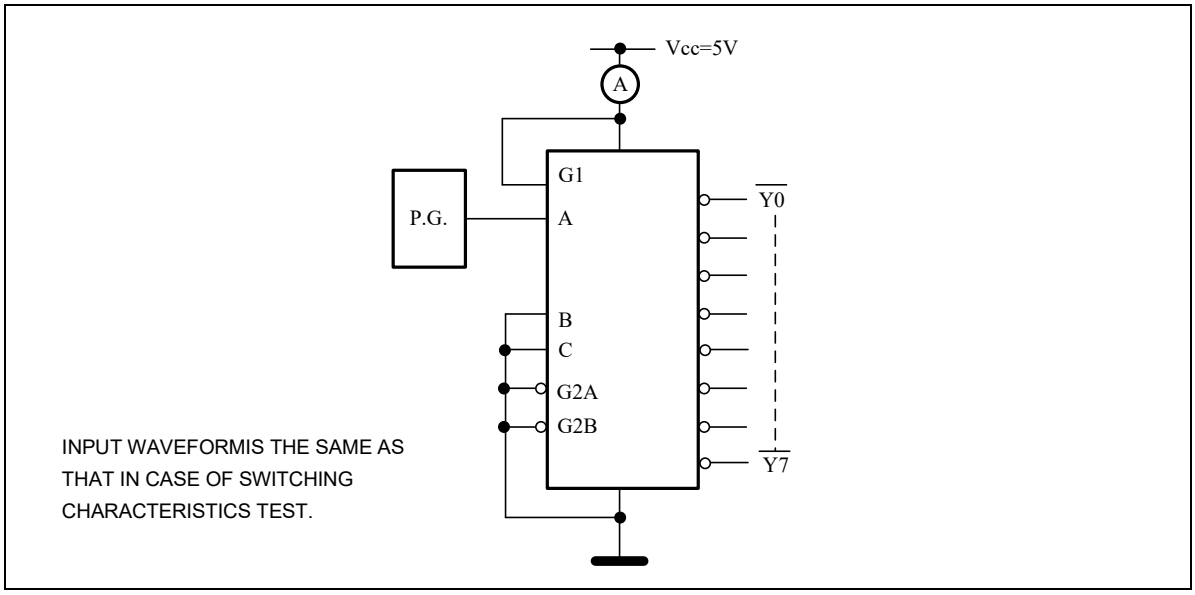
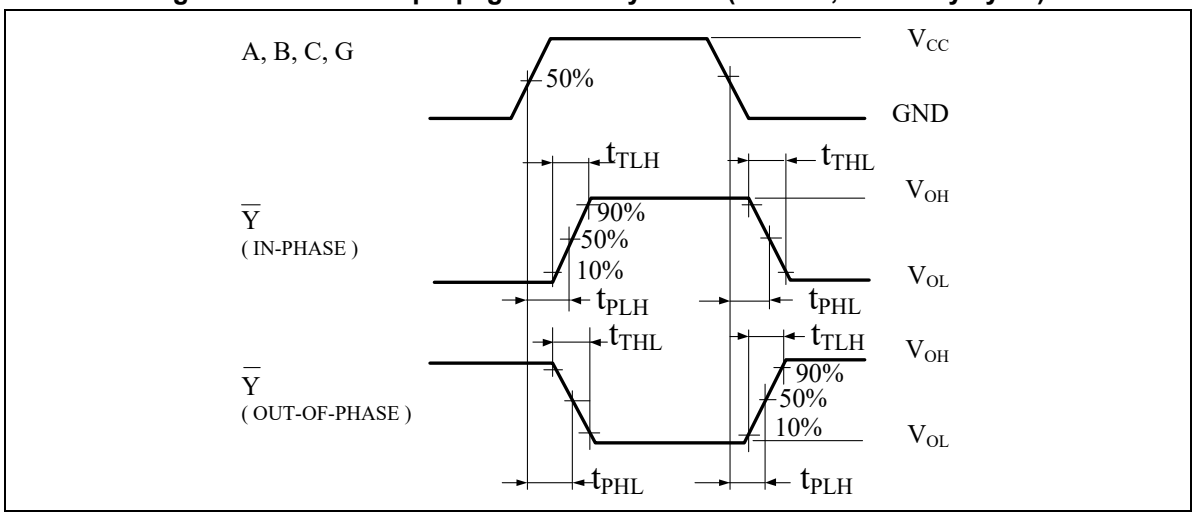
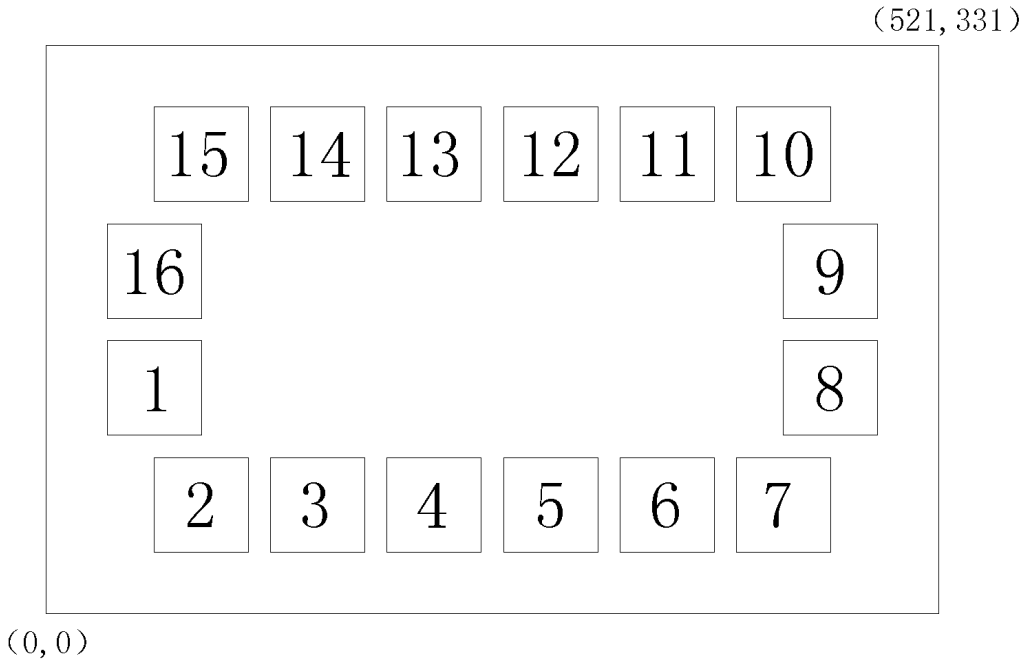


Figure 5. Waveform: propagation delay times (f=1MHz; 50% duty cycle)



6 Die Information

Die Type	RD74HC138	Wafer Size	8 Inch
Die Size (μm)	X/Y:521/331	Bond Area (μm)	X/Y: 55/55
Scribeline (μm)	60	Chip Thickness	
Metal	Front	Al+0.5%Cu	
	Back	Si	
	Top Metal Thickness	12000Å	



Pin No.	Pin Name	Coordinate			Pin No.	Pin Name	Coordinate	
		X	Y				X	Y
1	A	63.5	131.5		9	$\overline{Y6}$	440.5	199.5
2	B	73.5	63.5		10	$\overline{Y5}$	413.5	267.5
3	C	141.5	63.5		11	$\overline{Y4}$	345.5	267.5
4	$\overline{G2A}$	209.5	63.5		12	$\overline{Y3}$	277.5	267.5
5	$\overline{G2B}$	277.5	63.5		13	$\overline{Y2}$	209.5	267.5
6	$\overline{G1}$	345.5	63.5		14	$\overline{Y1}$	141.5	267.5
7	$\overline{Y7}$	413.5	63.5		15	$\overline{Y0}$	73.5	267.5
8	GND	440.5	131.5		16	V_{CC}	63.5	199.5

7 Ordering information

Table 12. Device summary

Order code	Package	Packing
RD74HC138BDI	DIP16	Tape and reel
RD74HC138BSO	SOP16	
RD74HC138BTS	TSSOP16	
RD74HC138B		Wafer

8 Revision history

Table 13. Document revision history(1)

Date	Revision	Changes
18-Jan-2022	1	Initial release
12-Dec-2023	2	Added : Die information Revised document presentation, minor textual updates

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