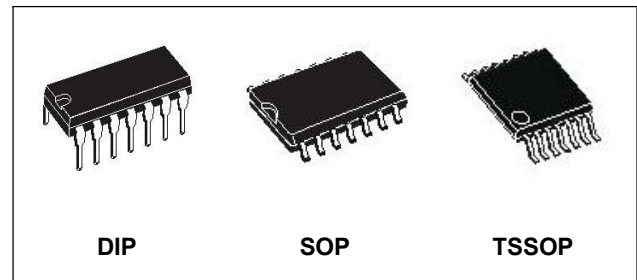


QUAD 2-INPUT NAND GATE

Datasheet- production data

Features

- HIGH SPEED:
 $t_{PD} = 8\text{ns}$ (TYP.) at $V_{CC} = 6\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 1\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4\text{mA}$ (MIN.)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 $V_{CC}(\text{OPR.}) = 2\text{V to } 6\text{V}$



The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Description

The RD74HC00 is a high-speed CMOS QUAD 2-INPUT NAND GATE fabricated with silicon gate CMOS technology.

Table 1. Device summary

PART NUMBER	PACKAGE
RD74HC00BDI	DIP14
RD74HC00BSO	SOP14
RD74HC00BTS	TSSOP14

1 Pin information

Figure 1. Pin connection and IEC logic symbols

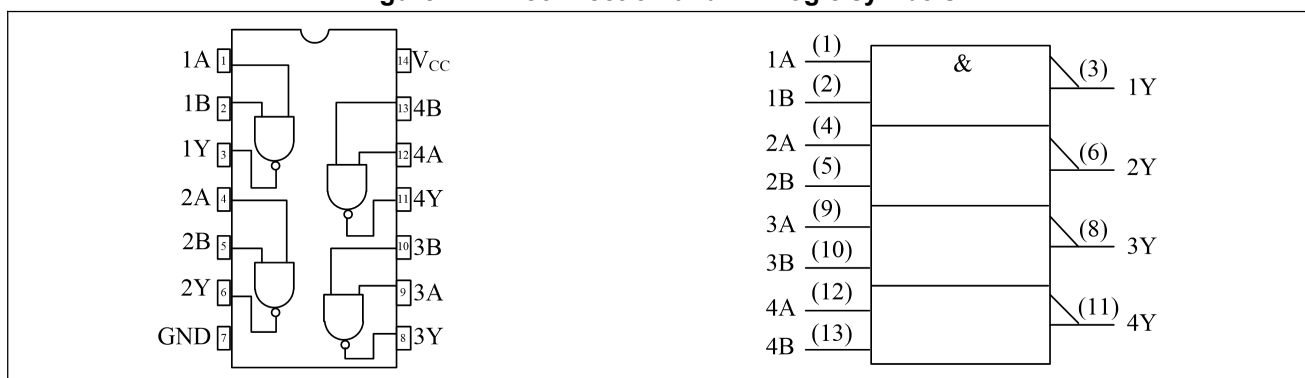


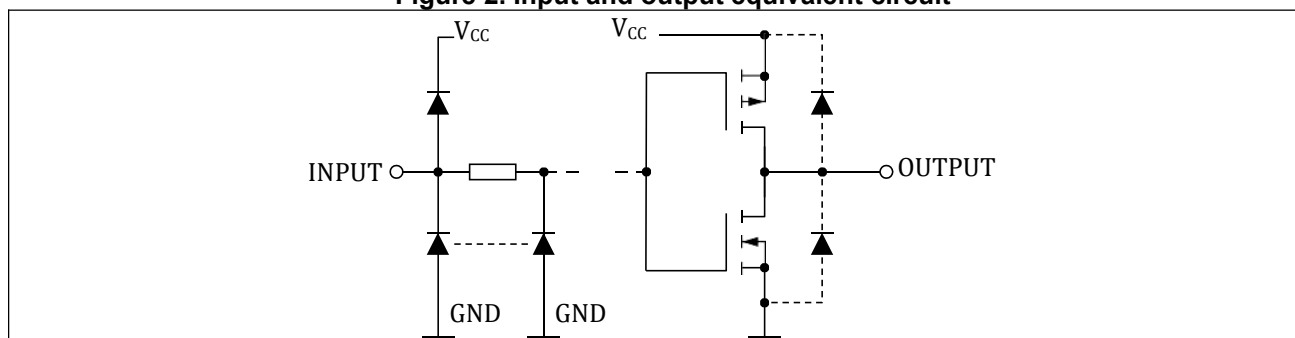
Table 2. Pin description

Pin No	Symbol	Name and function
1,4,9,12	1A to 4A	Data Inputs
2, 5, 10,13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V _{CC}	Positive Supply Voltage

2 Functional description

Table 3. Truth table

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Figure 2. Input and output equivalent circuit

3 Absolute maximum ratings and operating conditions

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to + 7.0	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to + 150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	2 to 6	V	
V_I	Input Voltage	0 to V_{CC}	V	
V_O	Output Voltage	0 to V_{CC}	V	
T_{op}	Operating Temperature	-40 to +85	°C	
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		$T_A = 25^\circ C$			-40 to $85^\circ C$		
				Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		V
		4.5		3.15			3.15		
		6.0		4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5	V
		4.5				1.35		1.35	
		6.0				1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	$I_O = -20\mu A$	1.9	2.0		1.9		V
		4.5	$I_O = -20\mu A$	4.4	4.5		4.4		
		6.0	$I_O = -20\mu A$	5.9	6.0		5.9		
		4.5	$I_O = -4.0$ mA	4.18	4.31		4.13		
		6.0	$I_O = -5.2$ mA	5.68	5.8		5.63		
V_{OL}	Low Level Output Voltage	2.0	$I_O = 20\mu A$		0.0	0.1		0.1	V
		4.5	$I_O = 20\mu A$		0.0	0.1		0.1	
		6.0	$I_O = 20\mu A$		0.0	0.1		0.1	
		4.5	$I_O = 4.0$ mA		0.17	0.26		0.33	
		6.0	$I_O = 5.2$ mA		0.18	0.26		0.33	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND			± 0.1		± 1	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND			1		10	μA

Table 7. AC electrical characteristics ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		$T_A = 25^\circ C$			-40 to $85^\circ C$		
				Min	Typ	Max	Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	2.0			30	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
t_{PLH}, t_{PHL}	Propagation Delay Time	2.0			27	75		95	ns
		4.5			9	15		19	
		6.0			8	13		16	

Table 8. Capacitive characteristics

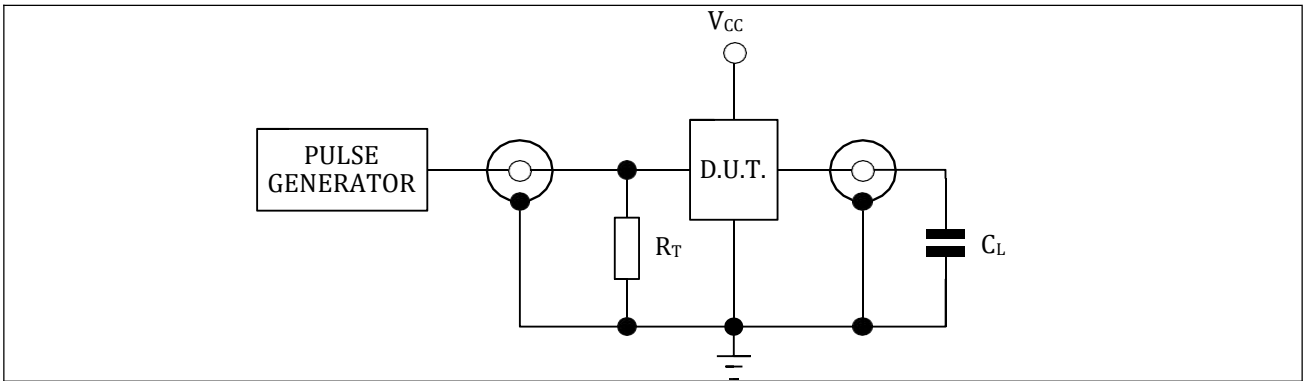
Symbol	Parameter	Test Condition		Value					Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
C _{IN}	Input Capacitance	5.0			5	10		10	pF
C _{PD}	Power Dissipation Capacitance ⁽¹⁾	5.0			20				pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation:

$$I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC} / 4(\text{per gate})$$

5 Test circuit

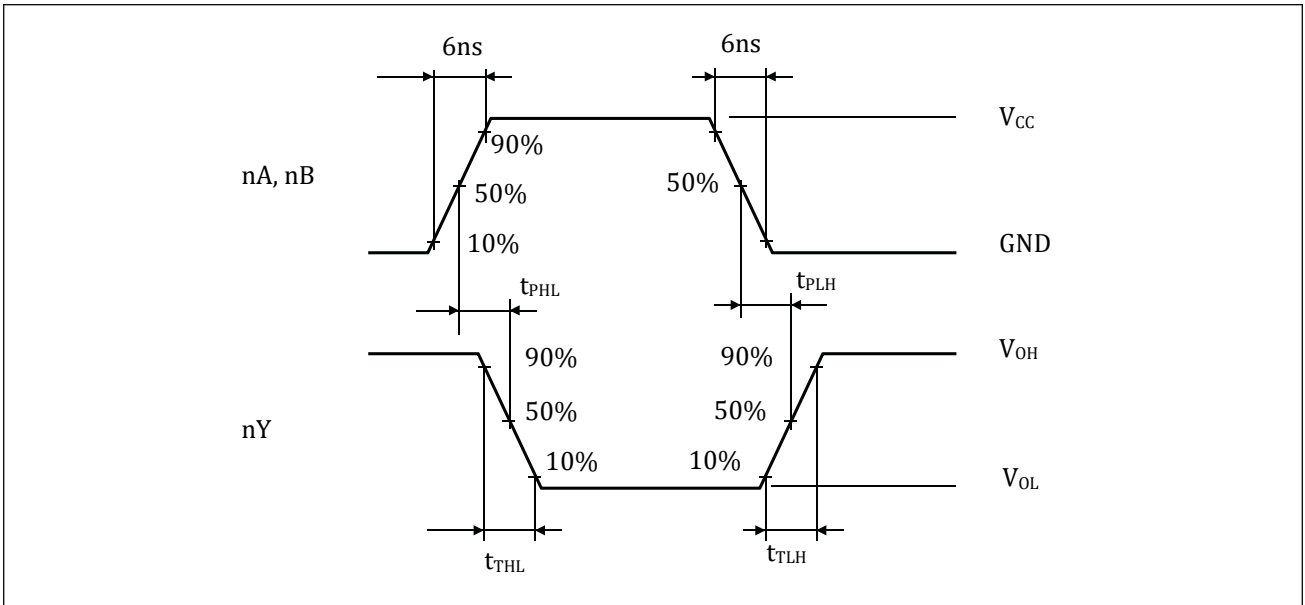
Figure 3. Test circuit



C_L = 50 pF or equivalent (includes jig and probe capacitance)

R_T = Z_{OUT} of pulse generator (typically 50Ω)

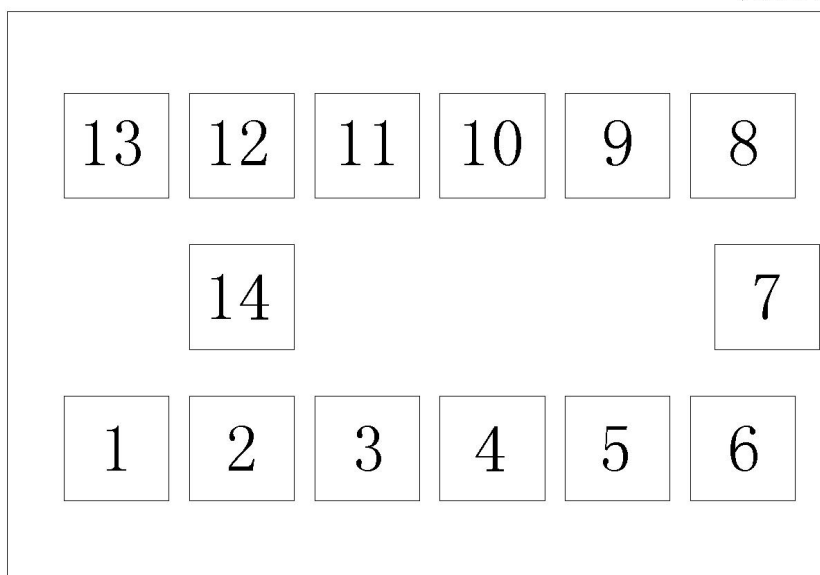
Figure 4. Waveform: propagation delay times (f=1 MHz; 50% duty cycle)



6 Die Information

Die Type		RD74HC00	Wafer Size	8 Inch
Die Size (μm)		X/Y:432.6/300	Bond Area (μm)	X/Y: 55/55
Scribeline (μm)		60	Chip Thickness	
Metal	Front		Al+0.5%Cu	
	Back		Si	
	Top Metal Thickness		12000Å	

(432.6, 300.0)



(0, 0)

Pin No.	Pin Name	Coordinate		Pin No.	Pin Name	Coordinate	
		X	Y			X	Y
1	1A	57.3	70.5	8	3Y	386.3	229.5
2	1B	123.1	70.5	9	3A	320.5	229.5
3	1Y	188.9	70.5	10	3B	254.7	229.5
4	2A	254.7	70.5	11	4Y	188.9	229.5
5	2B	320.5	70.5	12	4A	123.1	229.5
6	2Y	386.3	70.5	13	4B	57.3	229.5
7	GND	398.95	150.0	14	V _{CC}	123.1	150.0

7 Ordering information

Table 9. Device summary

Order code	Package	Packing
RD74HC00BDI	DIP14	Tape and reel
RD74HC00BSO	SOP14	
RD74HC00BTS	TSSOP14	
RD74HC00B		Wafer

8 Revision history

Table 10. Document revision history⁽¹⁾

Date	Revision	Changes
18-Jan-2022	1	Initial release
12-Dec-2023	2	Added : Die information Revised document presentation, minor textual updates

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